Fig.1

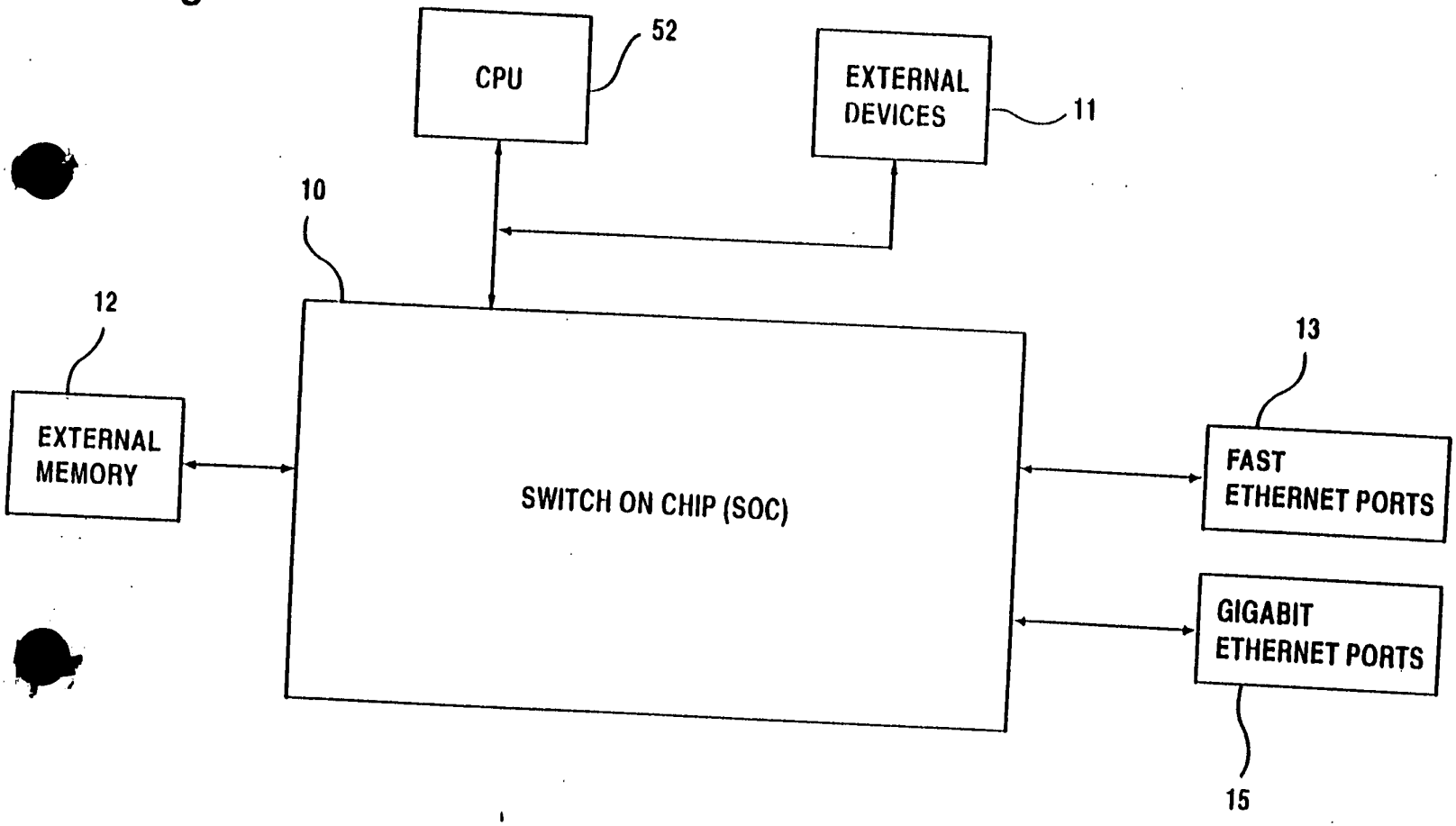


Fig.2

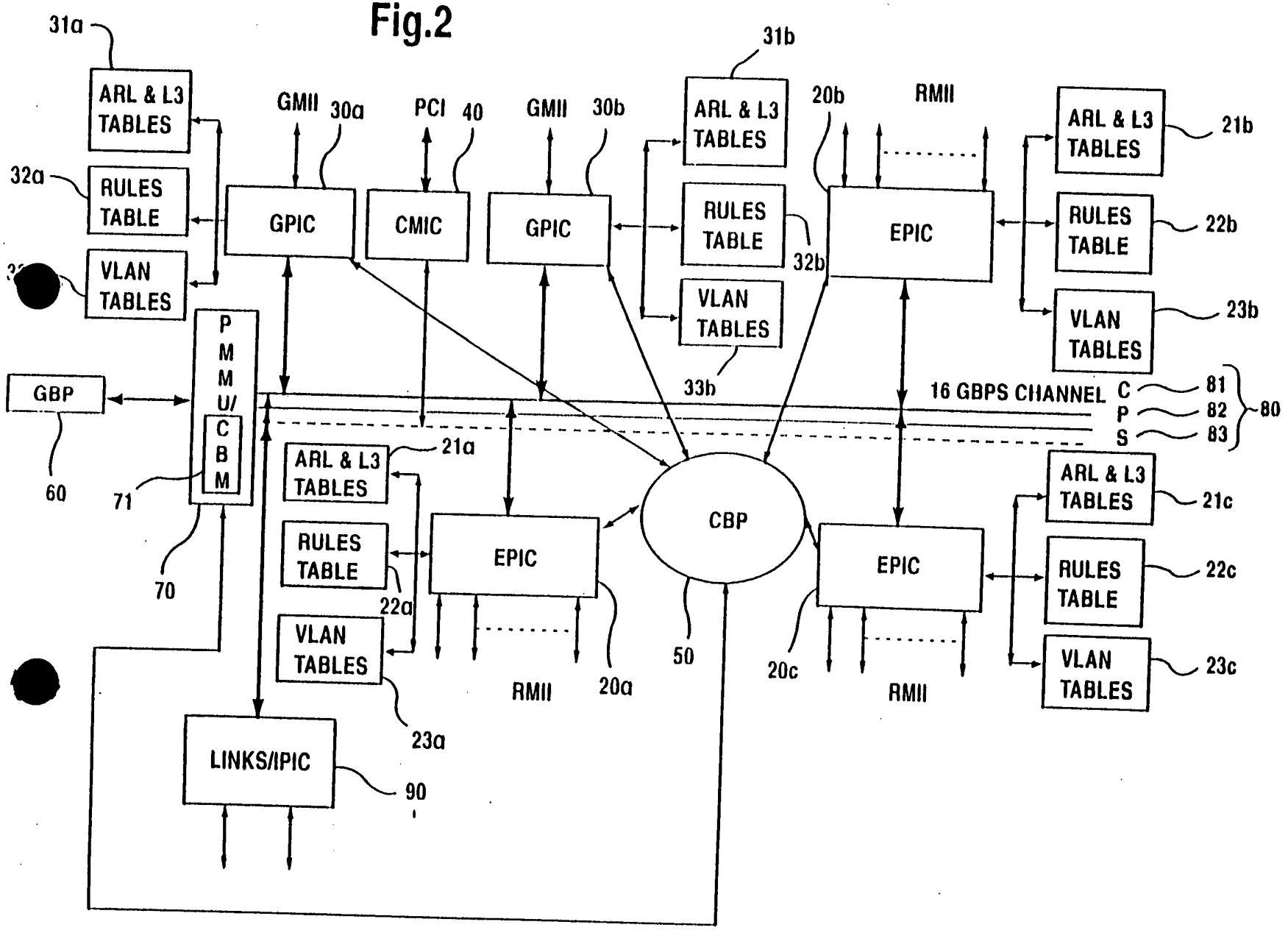


Fig.3

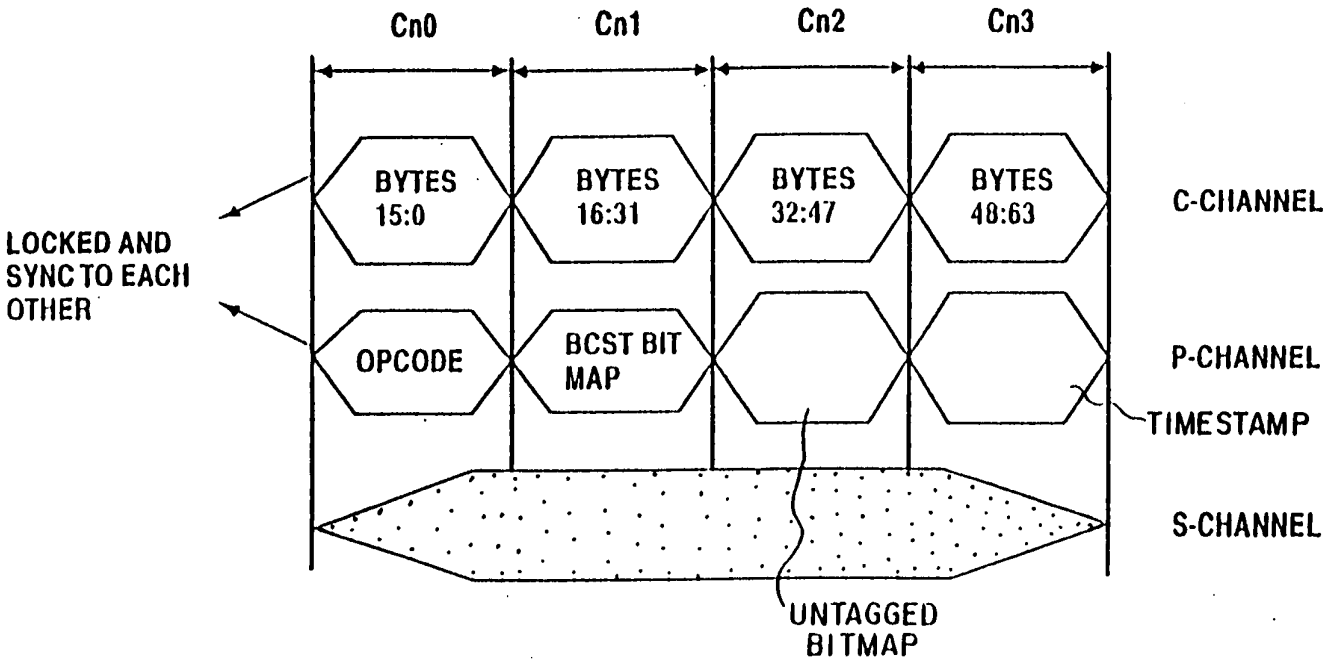


Fig.4a

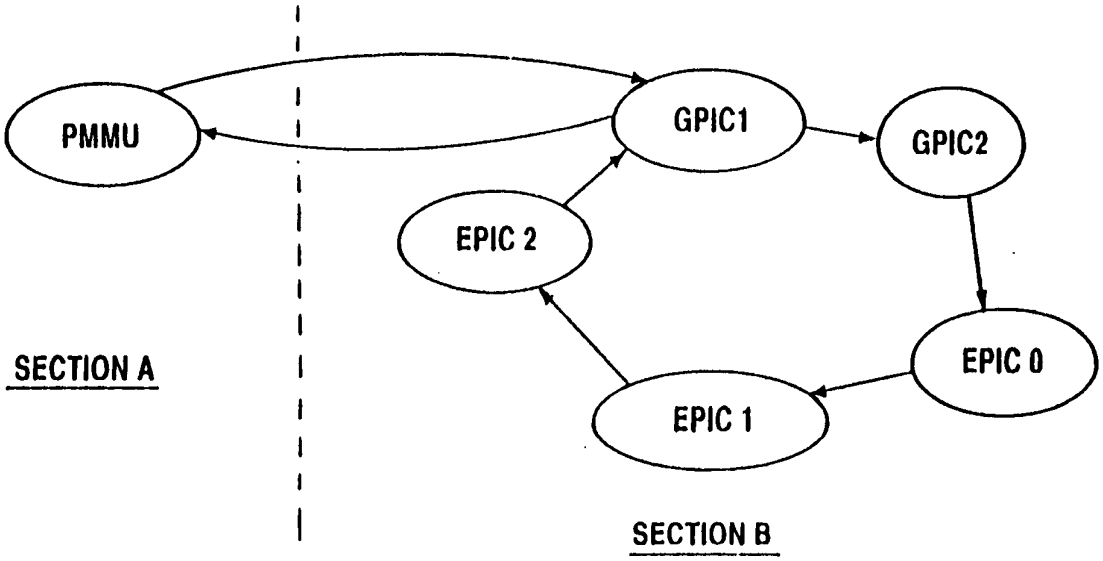


Fig.4b

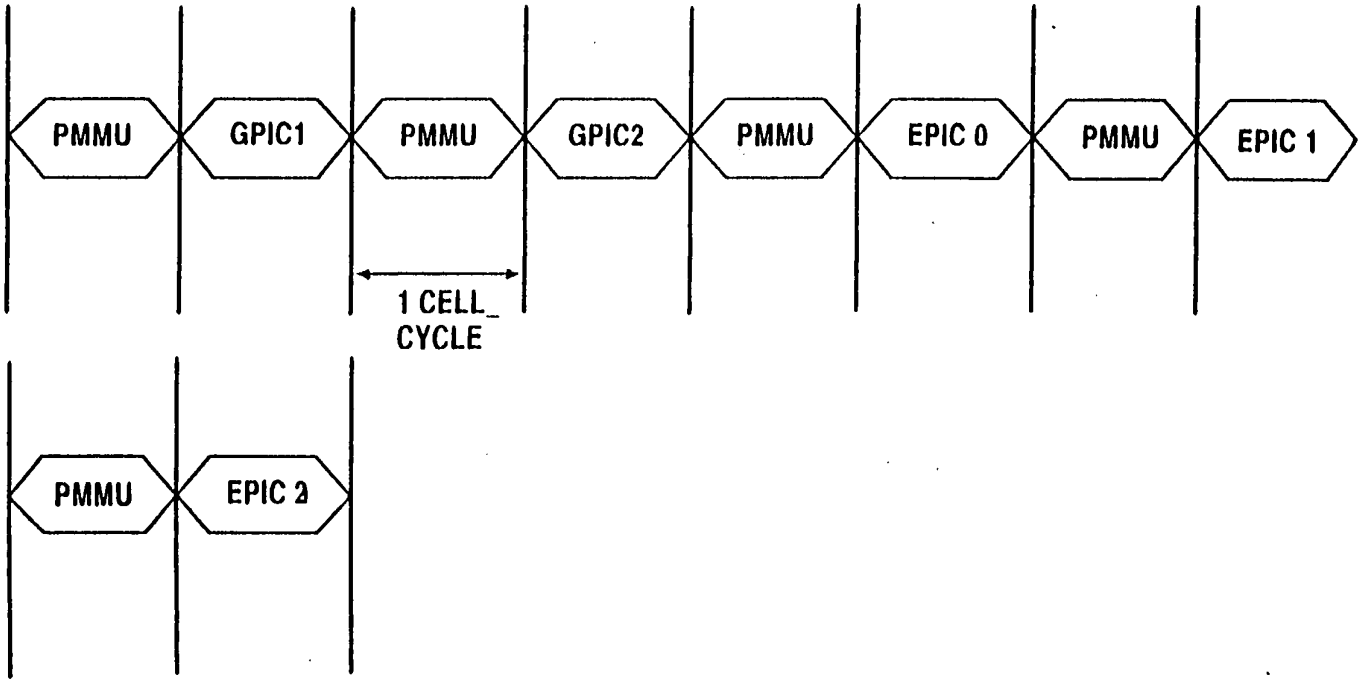


Fig.5

PROTOCOL CHANNEL MESSAGES

30	28		26	24	22	20	18	16	14	12		10	8		6	4	2	0
OP CODE	I P	I P X	RESERVED	NXT CELL	SRC DEST PORT			COS	J	S	E	CR C	P	O	LEN			

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
RESERVED	BC/MC PORTBITMAP														

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
U	RES	UNTAGGED PORTBITMAP/SRC PORT NUMBER (BIT0..5)													

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
CPU OPCODES									TIME STAMP						

Fig.6

SIDE BAND CHANNEL MESSAGES

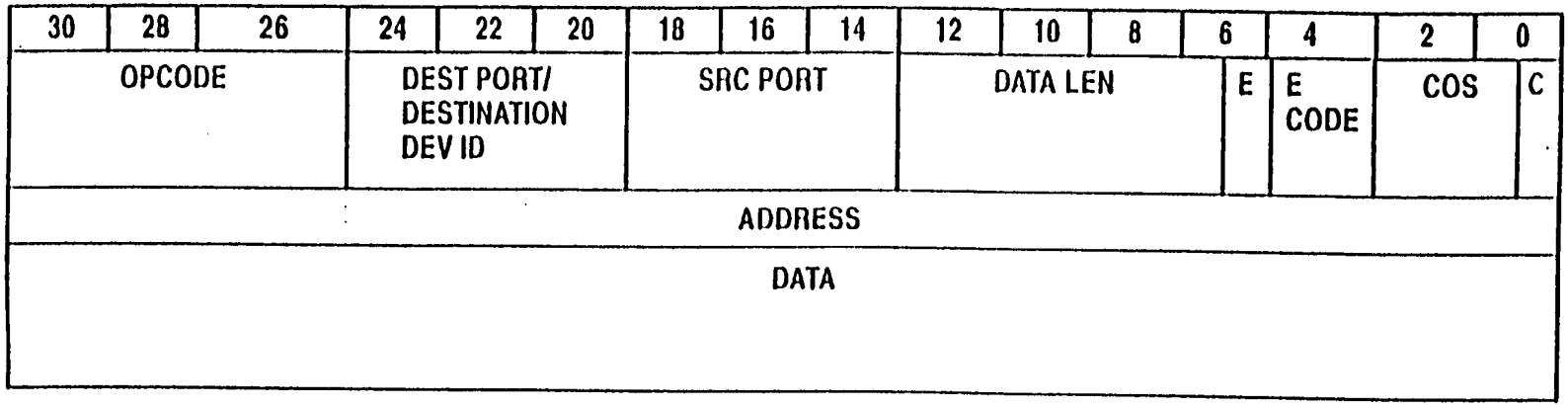


Fig.7
PRIOR ART

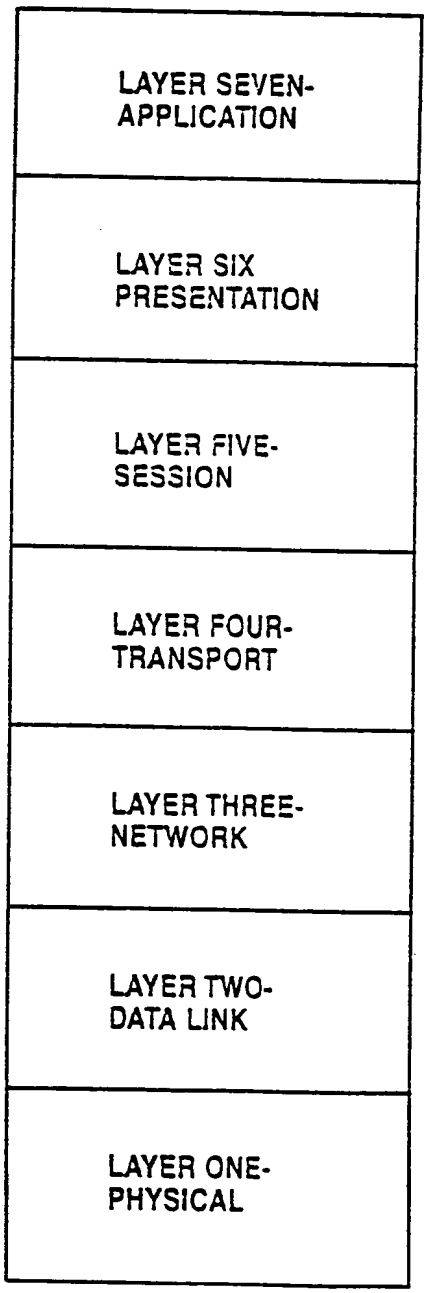


Fig.8

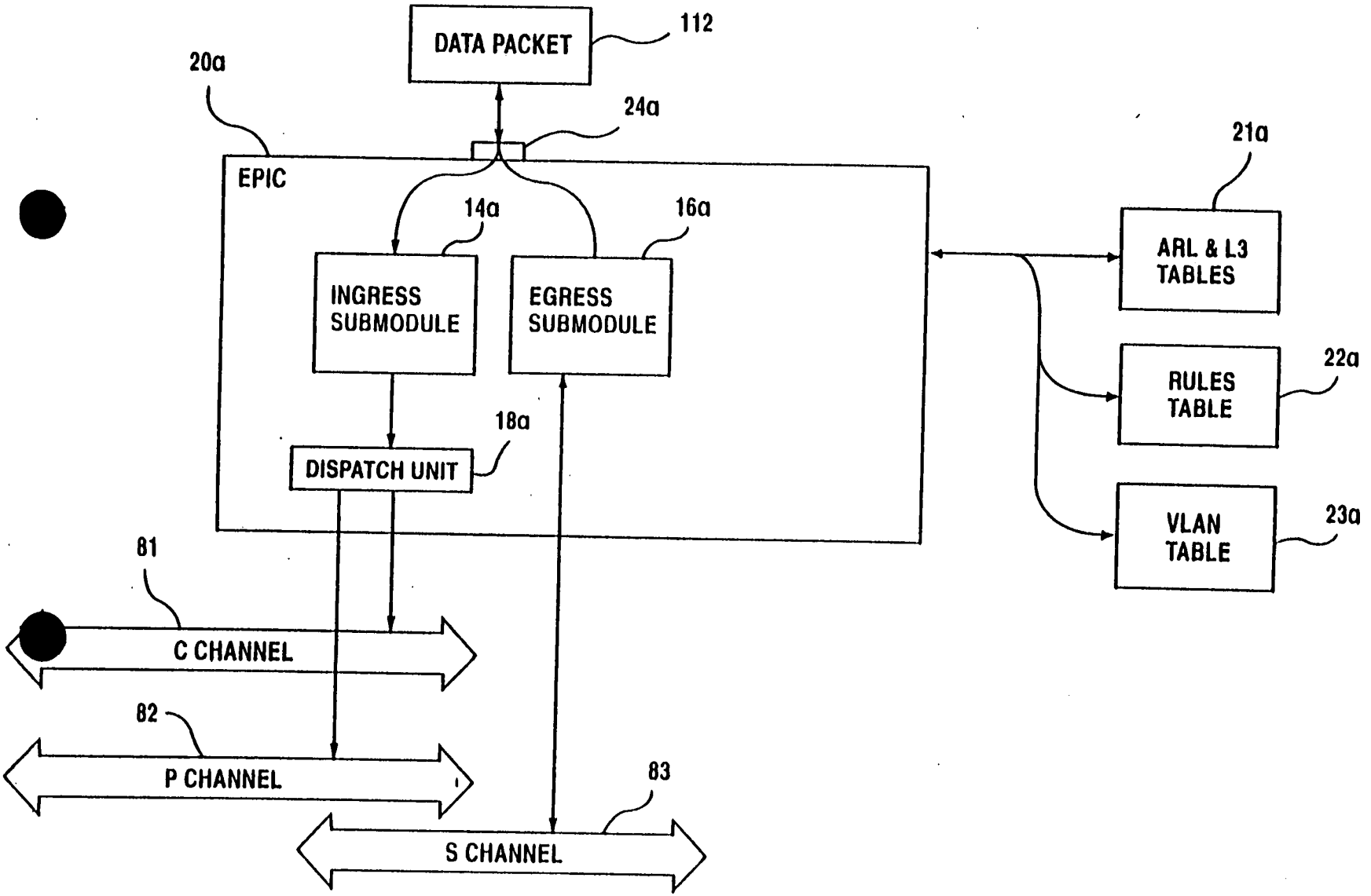


Fig.9

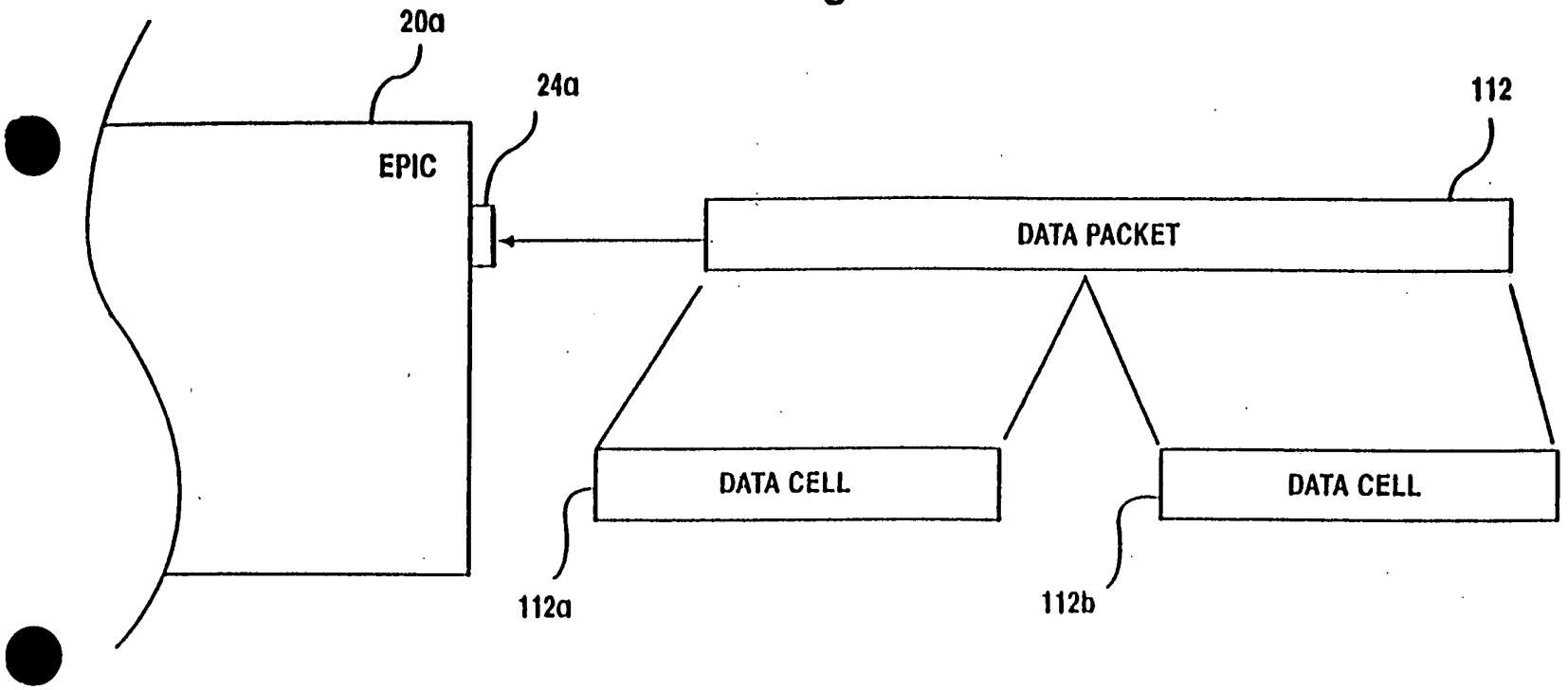


Fig.10

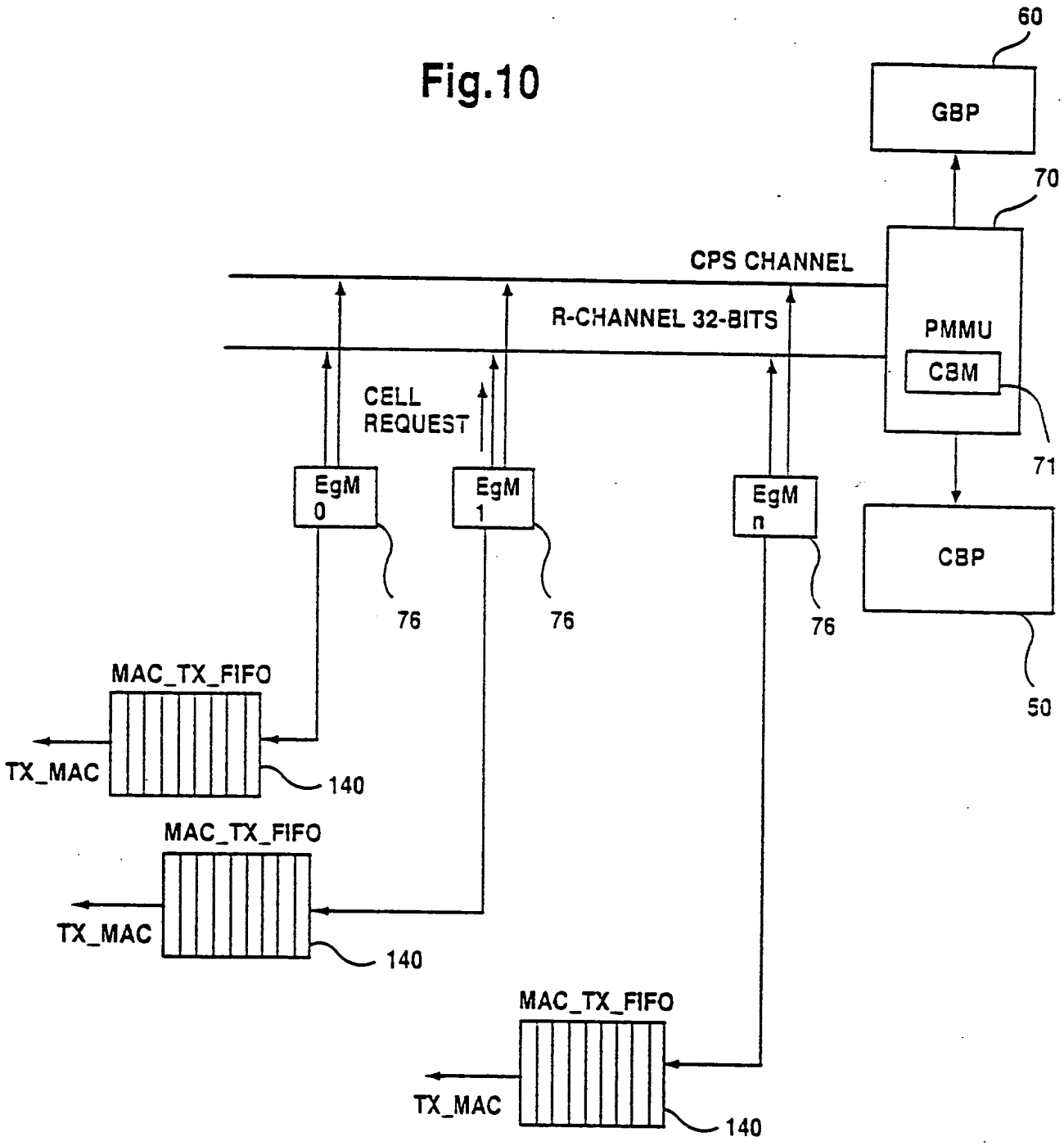

60
GBP
70
CPS CHANNEL
R-CHANNEL 32-BITS
PMMU
CBM
71
CELL
REQUEST
EgM
0
EgM
1
EgM
n
76
76
76
CBP
50
MAC_TX_FIFO
TX_MAC
140
MAC_TX_FIFO
TX_MAC
140
MAC_TX_FIFO
TX_MAC
140

Fig.11

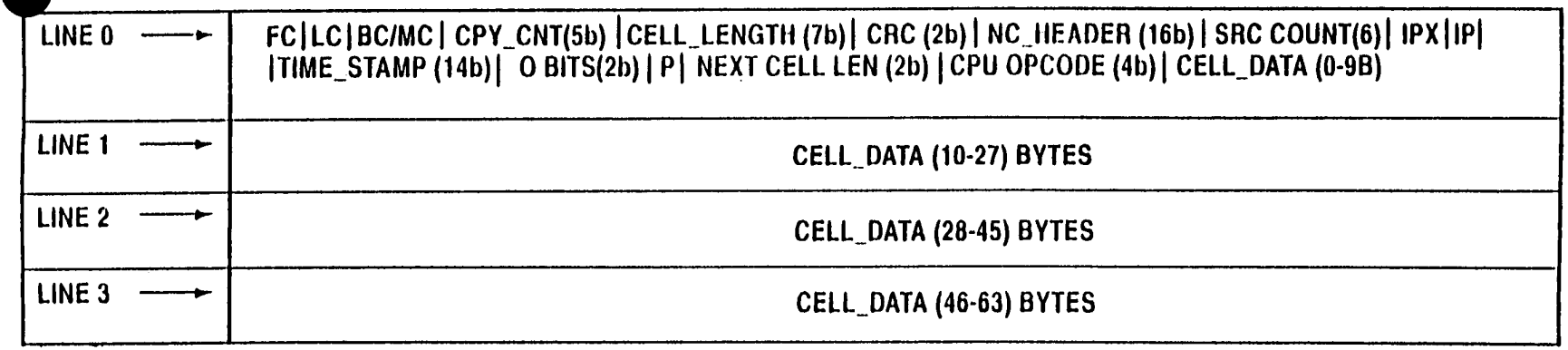


Fig.12

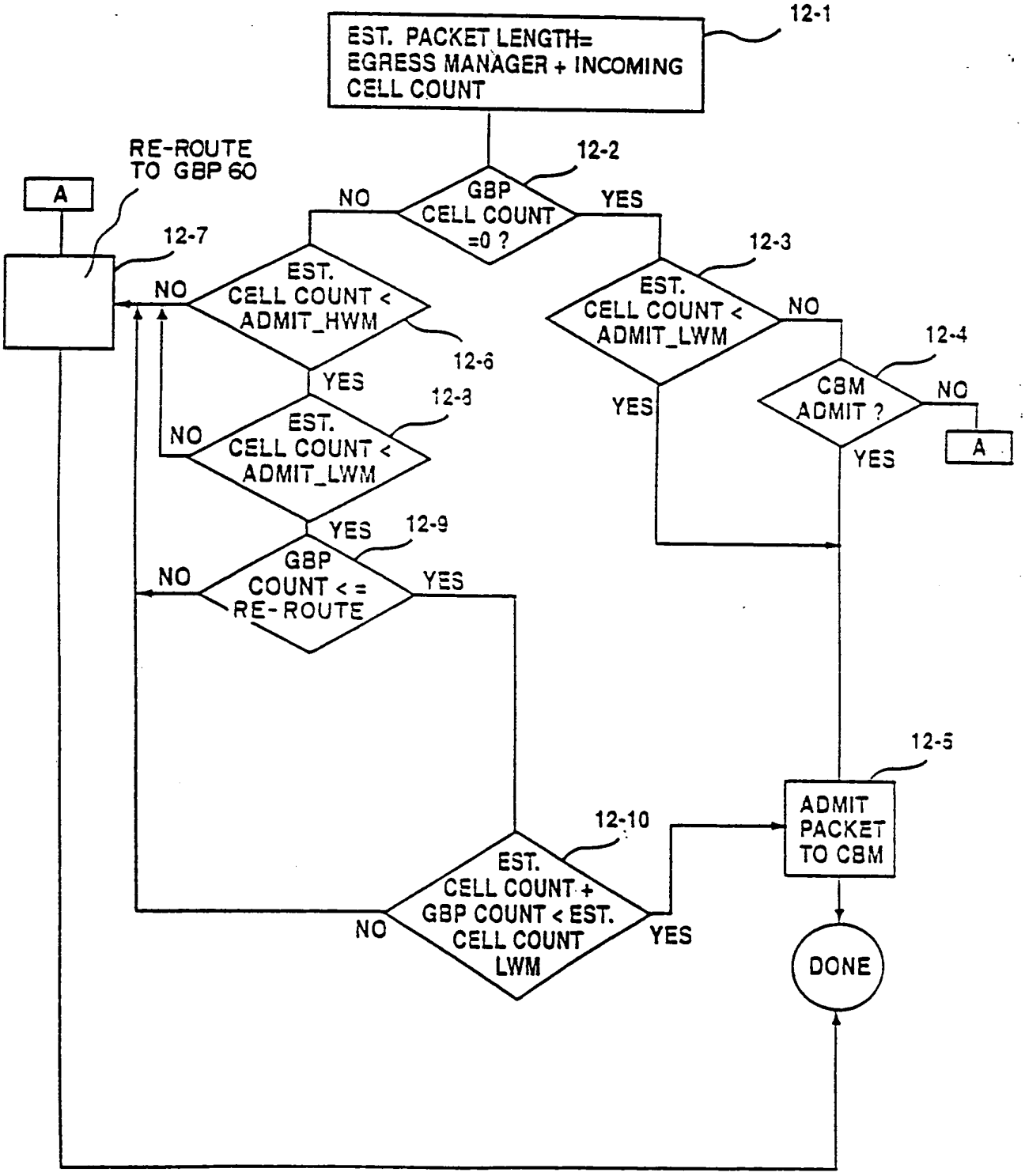

EST. PACKET LENGTH= EGRESS MANAGER + INCOMING CELL COUNT
12-1
GBP CELL COUNT =0 ?
12-2
NO
YES
RE-ROUTE TO GBP 60
A
12-7
EST. CELL COUNT < ADMIT_HWM
12-6
NO
YES
EST. CELL COUNT < ADMIT_LWM
12-8
NO
YES
GBP COUNT < = RE-ROUTE
12-9
NO
YES
EST. CELL COUNT < ADMIT_LWM
12-3
NO
YES
CBM ADMIT ?
12-4
NO
YES
A
ADMIT PACKET TO CBM
12-5
EST. CELL COUNT + GBP COUNT < EST. CELL COUNT LWM
12-10
NO
YES
DONE

Fig.13

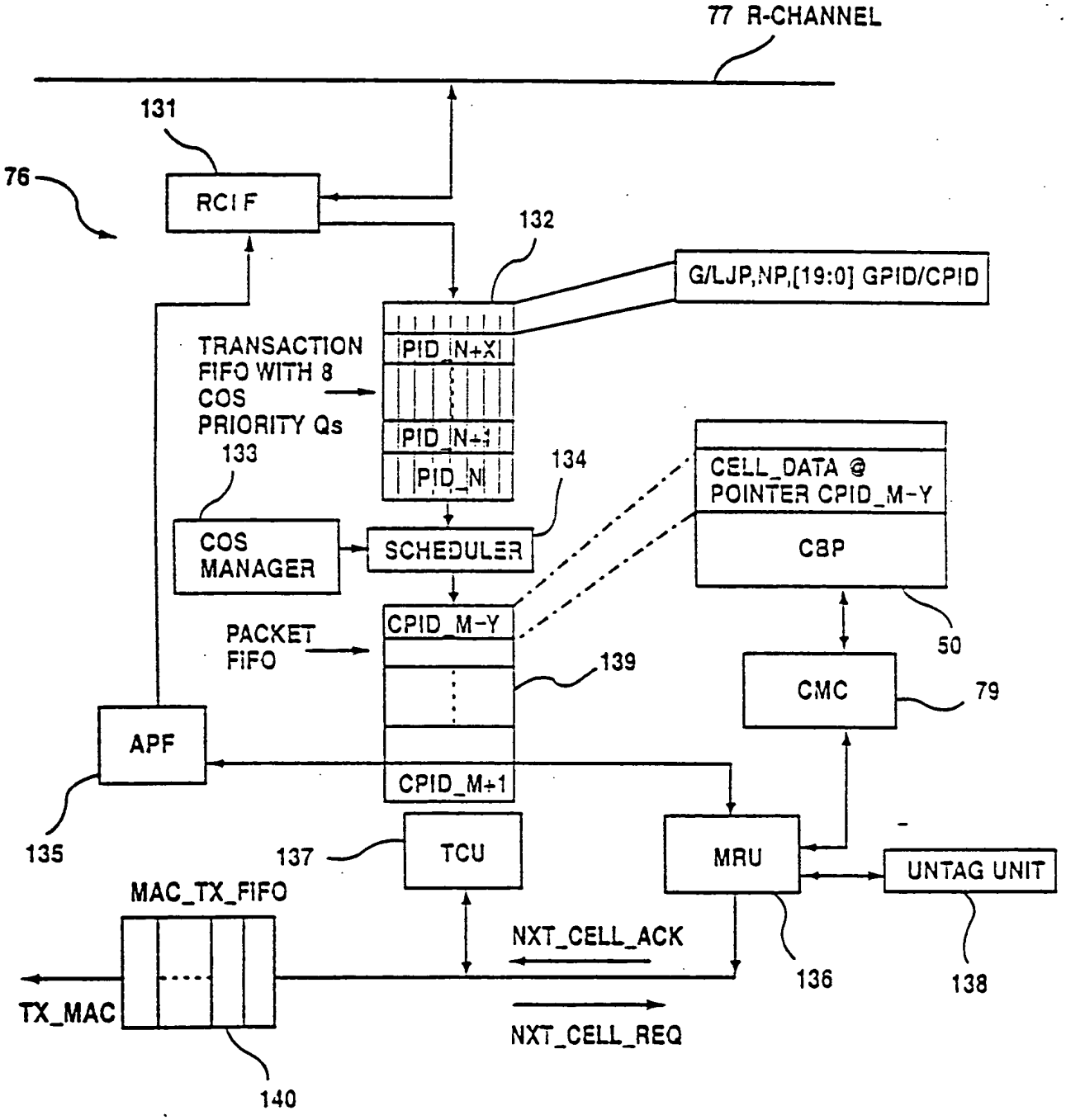

77 R-CHANNEL
131
76
RCIF
132
G/LJP,NP,[19:0] GPID/CPID
TRANSACTION FIFO WITH 8 COS PRIORITY Qs
PID_N+X
PID_N+1
PID_N
133
134
CELL_DATA @ POINTER CPID_M-Y
COS MANAGER
SCHEDULER
CBP
50
PACKET FIFO
CPID_M-Y
139
CMC
79
APF
CPID_M+1
135
137
TCU
MRU
UNTAG UNIT
MAC_TX_FIFO
NXT_CELL_ACK
136
138
TX_MAC
NXT_CELL_REQ
140

Fig.14

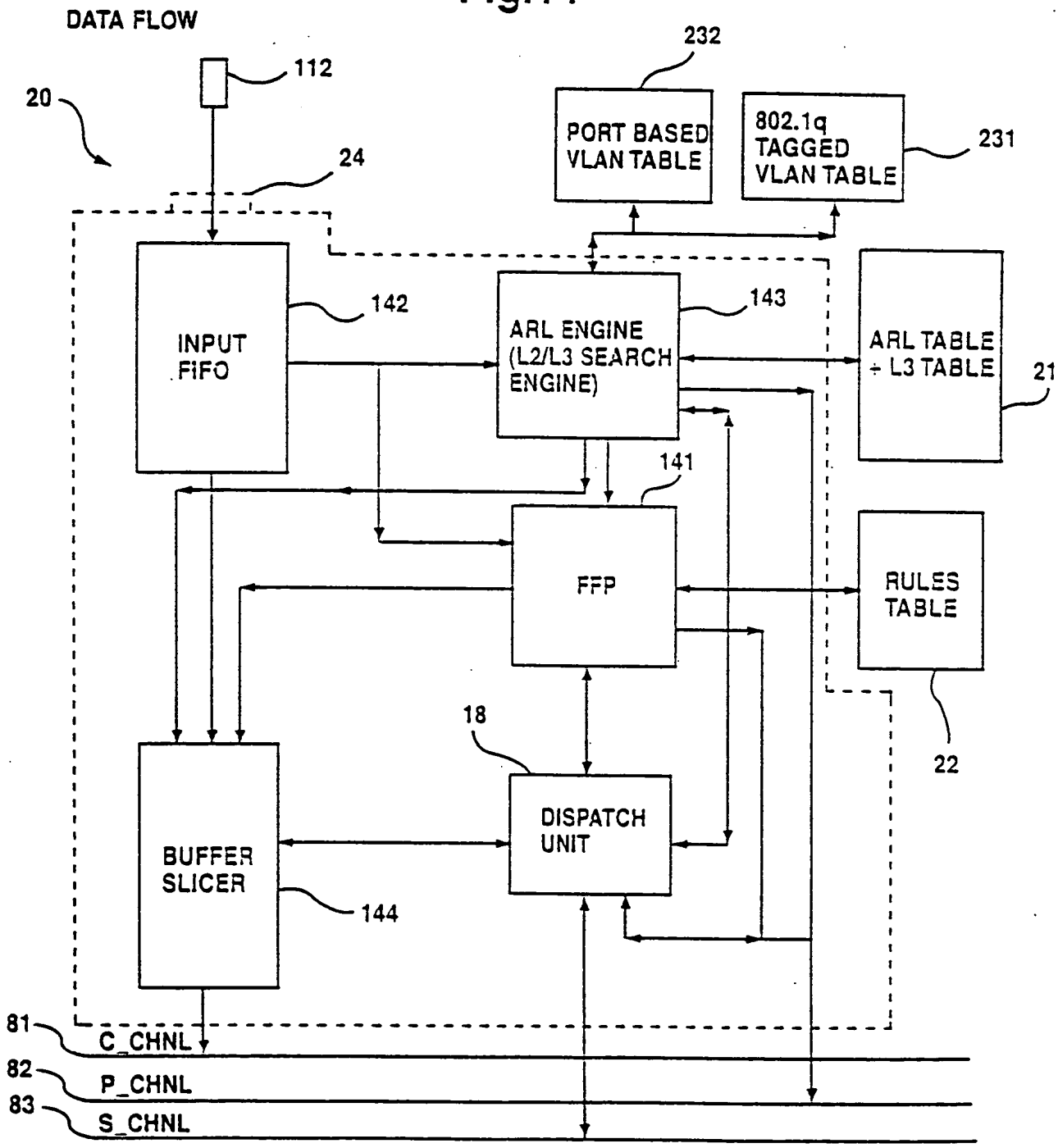

DATA FLOW
20
112
24
232
PORT BASED VLAN TABLE
802.1q TAGGED VLAN TABLE
231
INPUT FIFO
142
ARL ENGINE (L2/L3 SEARCH ENGINE)
143
ARL TABLE + L3 TABLE
21
141
FFP
RULES TABLE
22
18
DISPATCH UNIT
BUFFER SLICER
144
81
C_CHNL
82
P_CHNL
83
S_CHNL

Fig.15

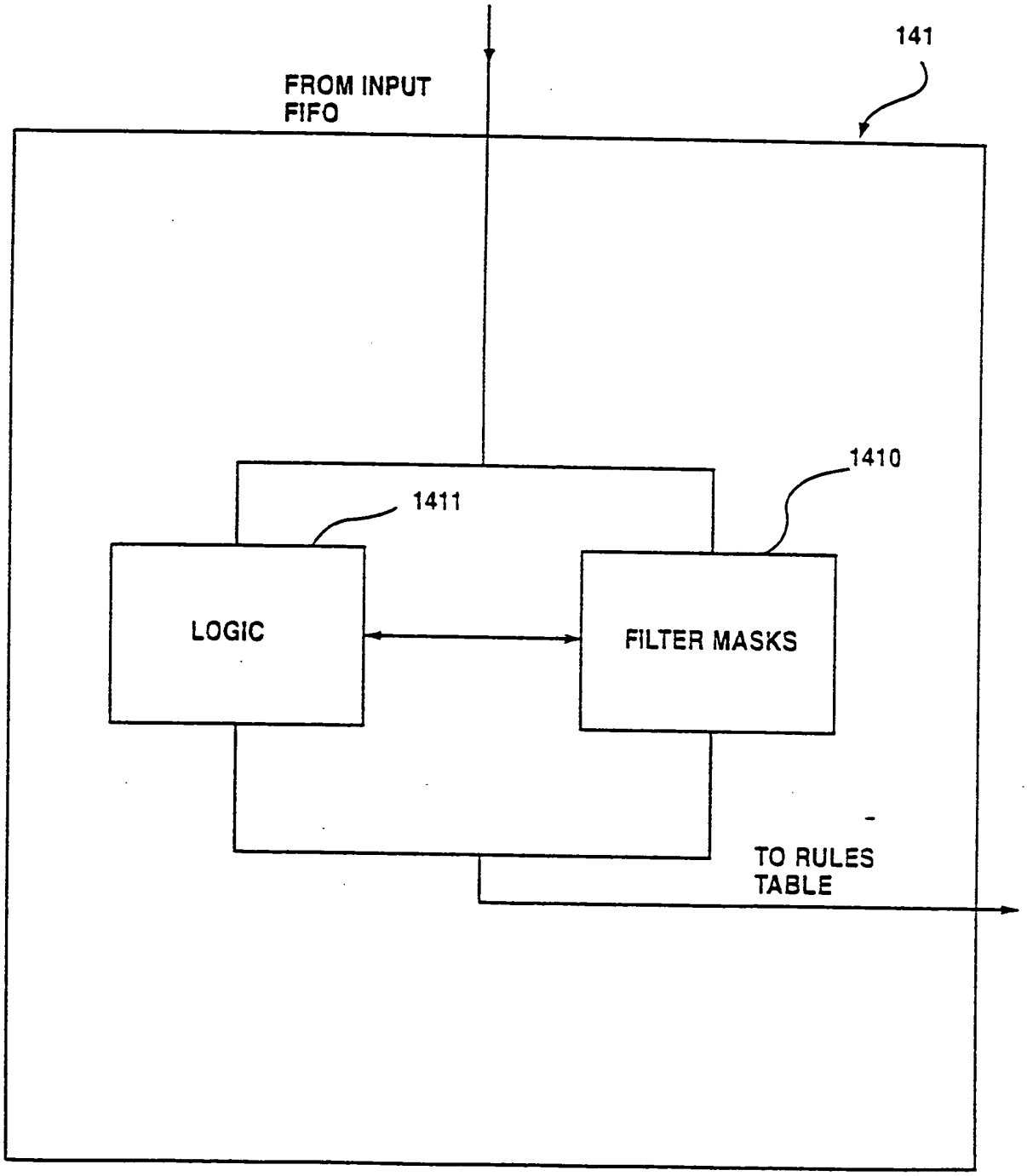

141
FROM INPUT
FIFO
1410
1411
LOGIC
FILTER MASKS
TO RULES
TABLE

Fig.16

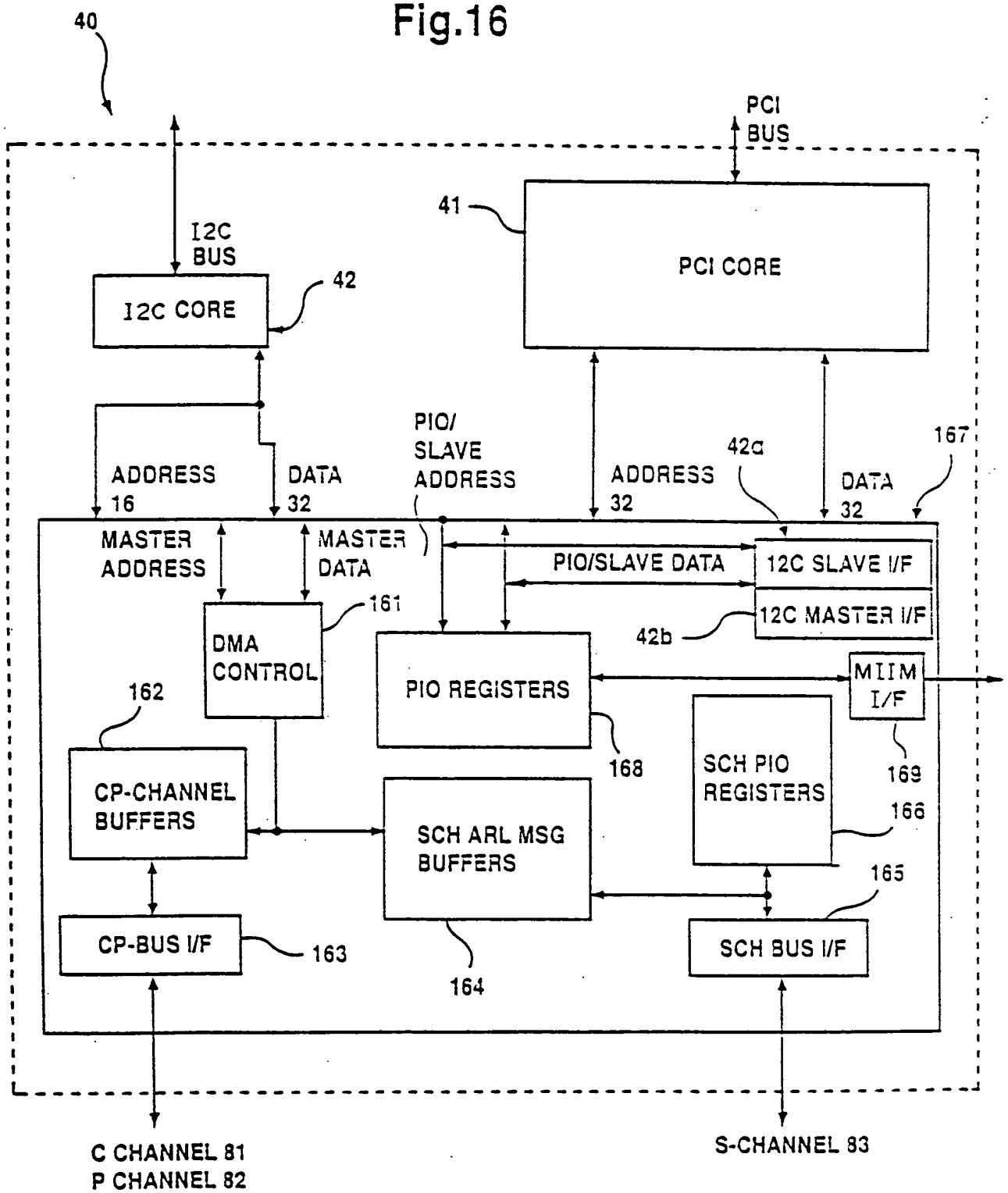

40
PCI BUS
41
PCI CORE
I2C BUS
I2C CORE
42
ADDRESS 16
DATA 32
PIO/ SLAVE ADDRESS
ADDRESS 32
42a
DATA 32
167
MASTER ADDRESS
MASTER DATA
PIO/SLAVE DATA
12C SLAVE I/F
12C MASTER I/F
42b
161
DMA CONTROL
PIO REGISTERS
MIIM I/F
162
168
169
CP-CHANNEL BUFFERS
SCH ARL MSG BUFFERS
SCH PIO REGISTERS
166
165
CP-BUS I/F
163
164
SCH BUS I/F
C CHANNEL 81
P CHANNEL 82
S-CHANNEL 83

Fig.17

FFP PROGRAMMING FLOW CHART

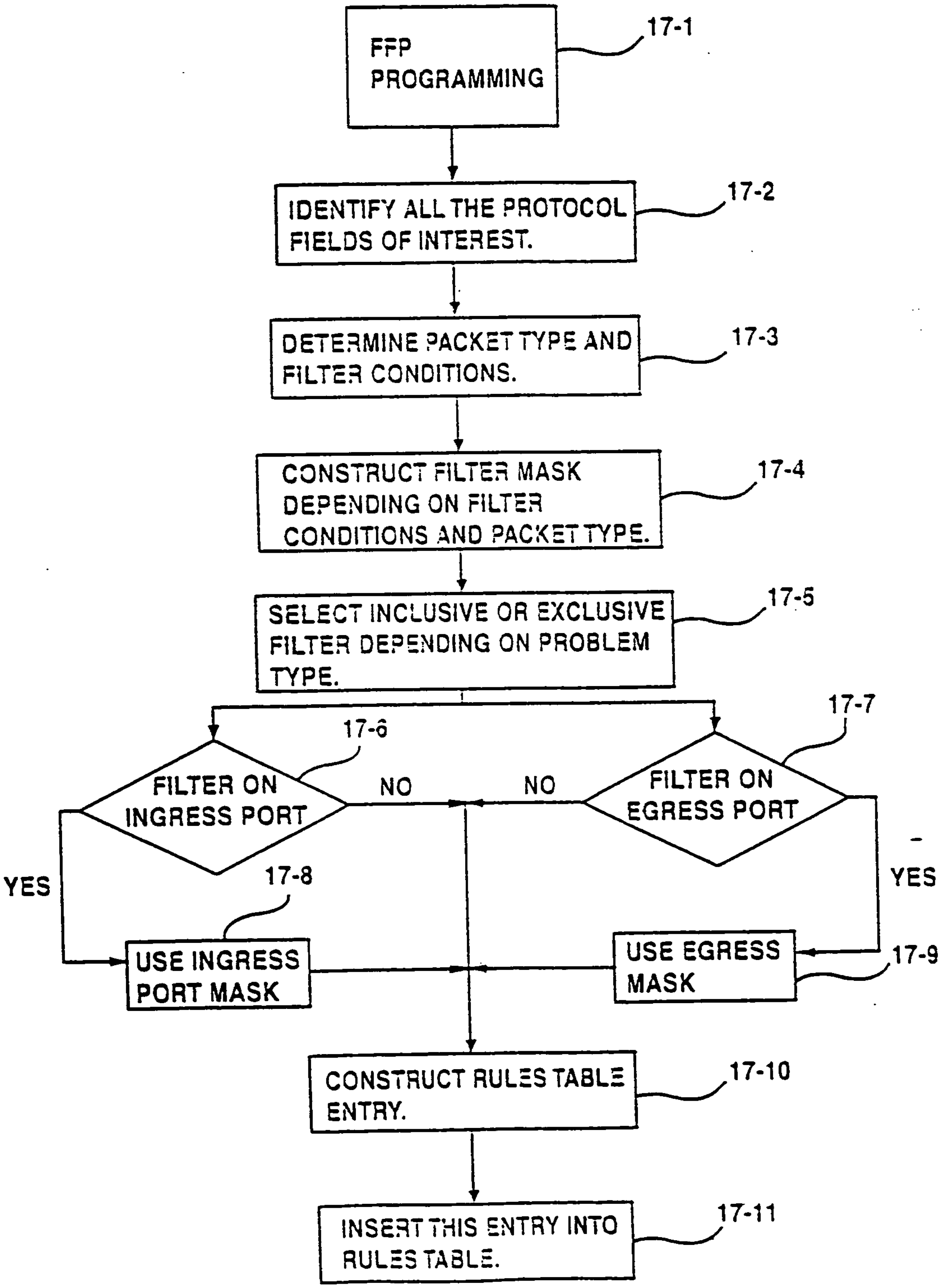


Fig.18

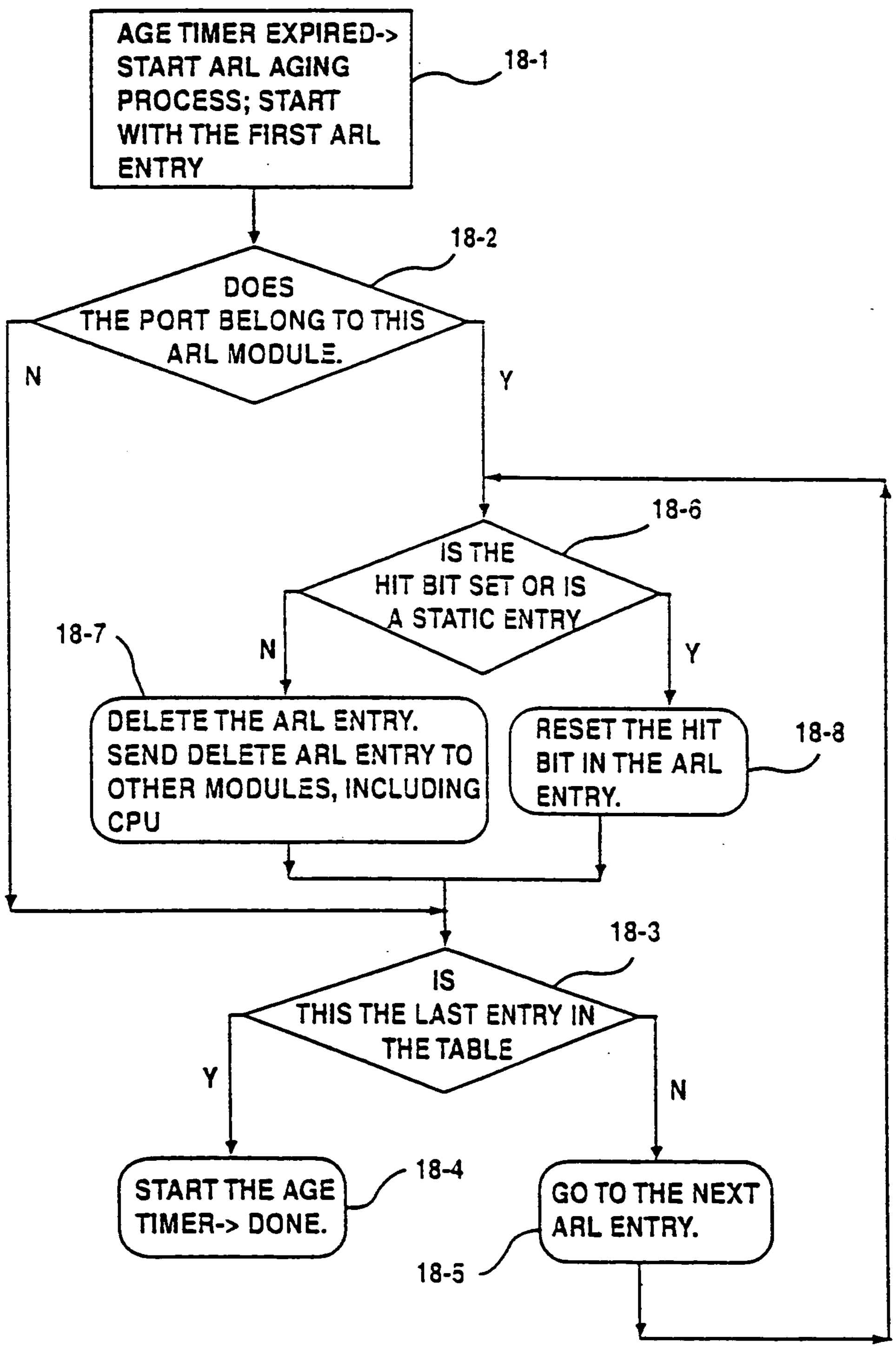
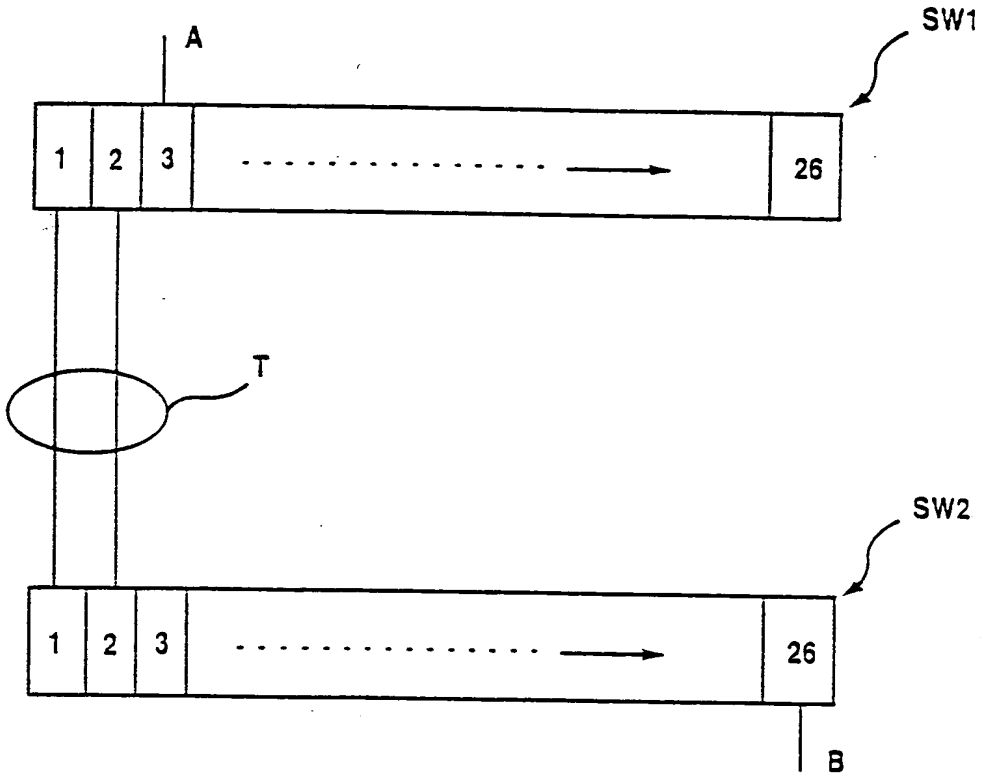


Fig.19



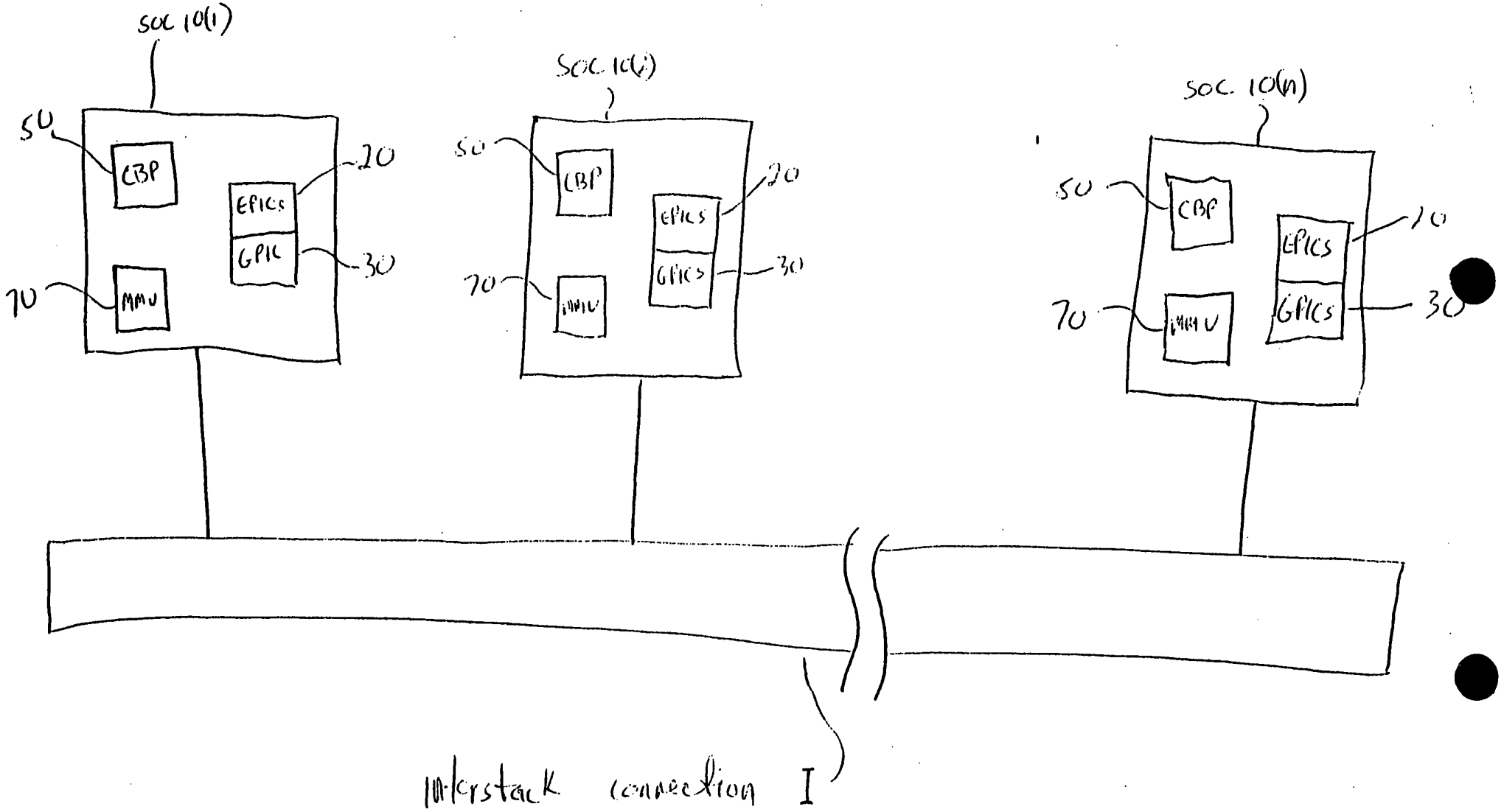

SOC 10(1)
SOC 10(2)
SOC 10(n)
50
CBP
20
EPICS
GPIC
30
70
MMU
Interstack connection I

Fig 20

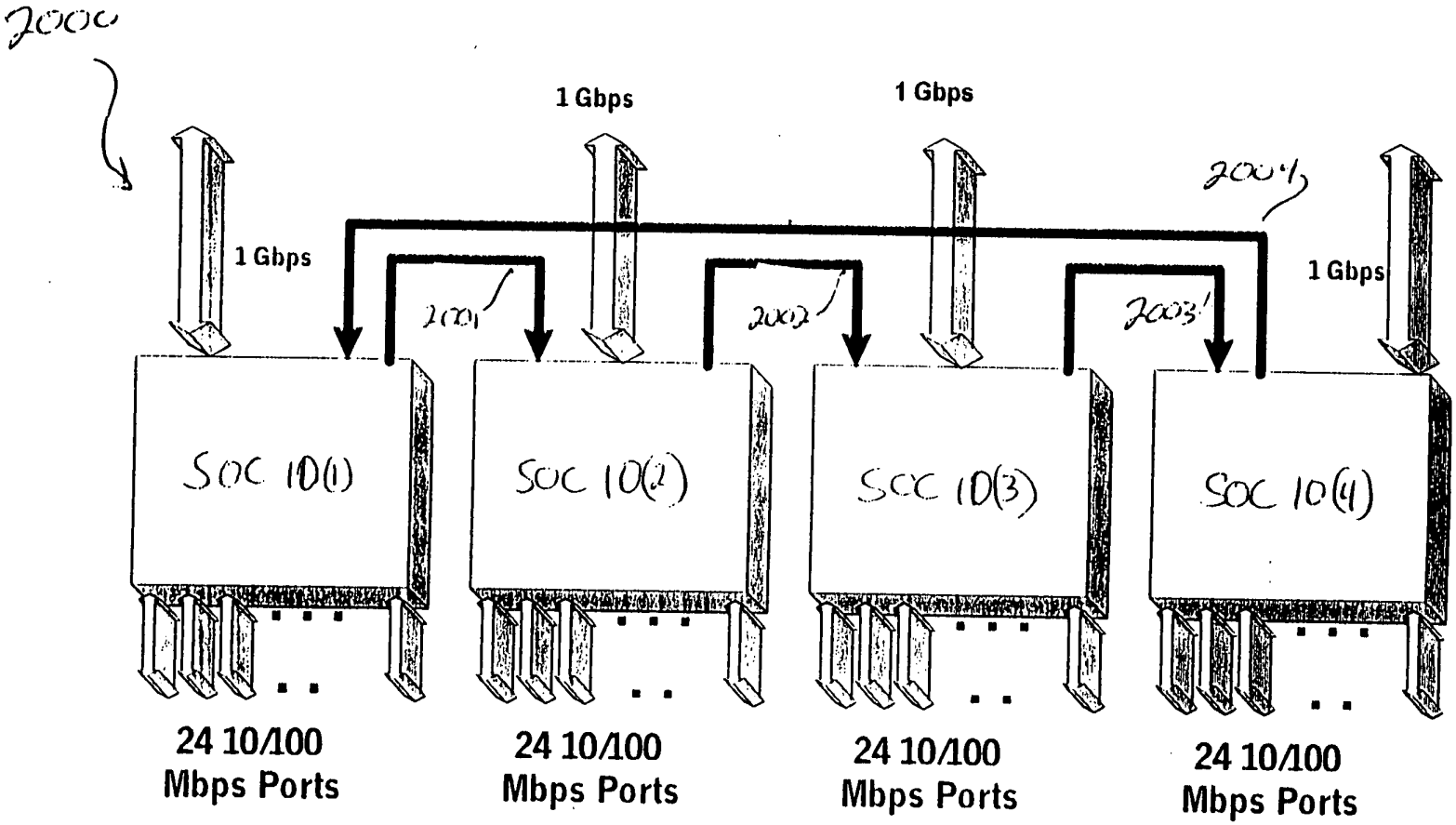


Fig. 21

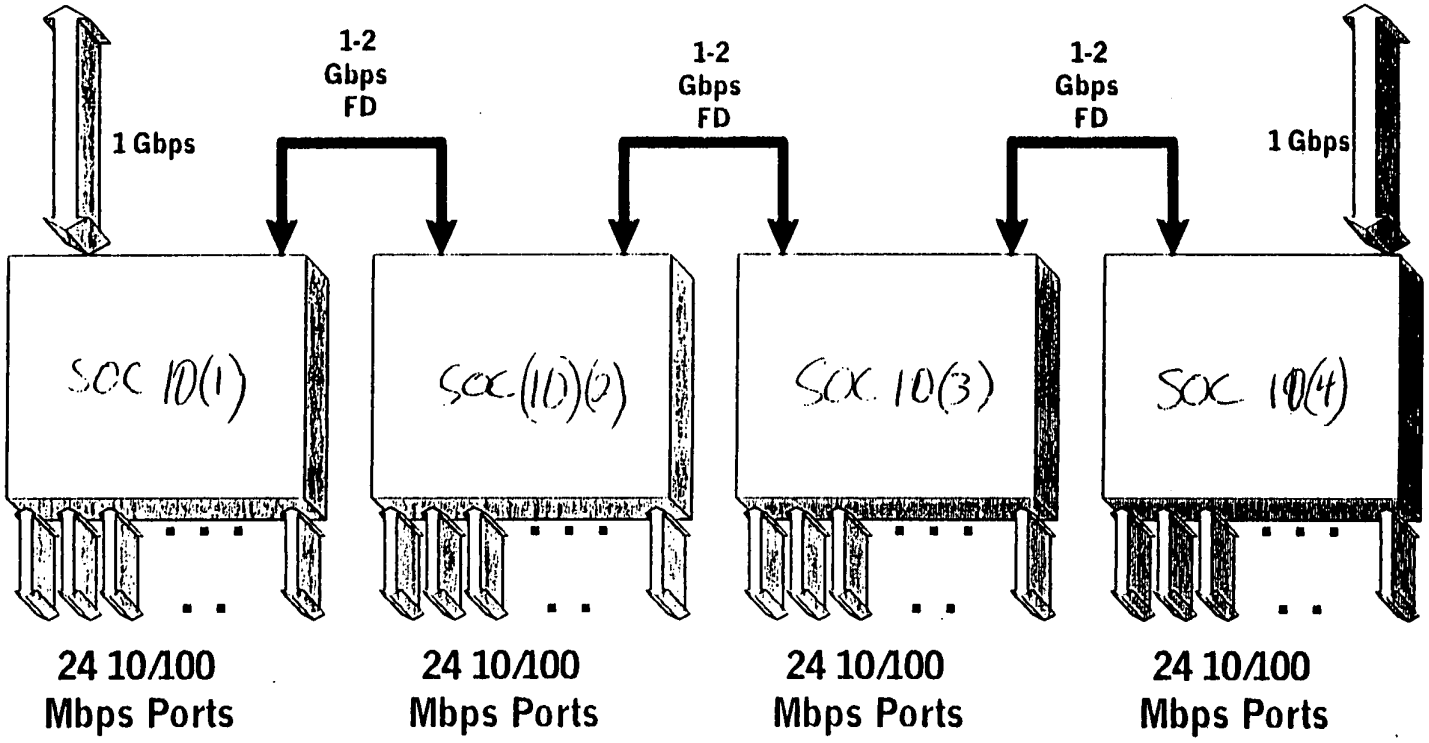


Fig. 22

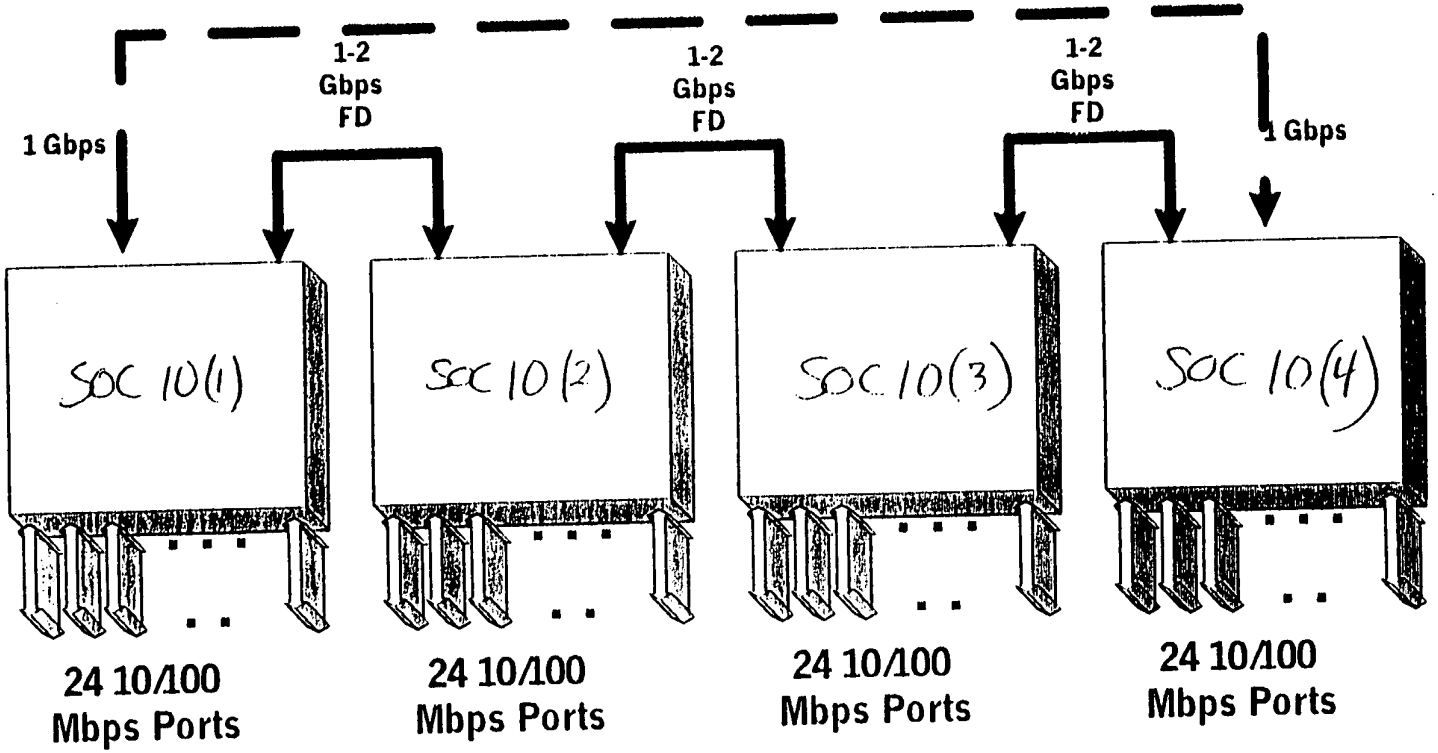


Fig. 23

112-S

IS

DA (6B)	SA (6B)	VLAN Tag (4B)	Stack Tag(4B)	Type/Len (2B)	Data

Fig. 24A

IS

Stack Count (5b)	SRC_ T (1b)	SRC_ TGID (3b)	SRC_ RTAG (3b)	DST_ T (1b)	DST_ TGID (3b)	DST_ RTAG (3b)	PFM (2b)	M (1b)	MD (1b)	Res (9)

Fig. 24B

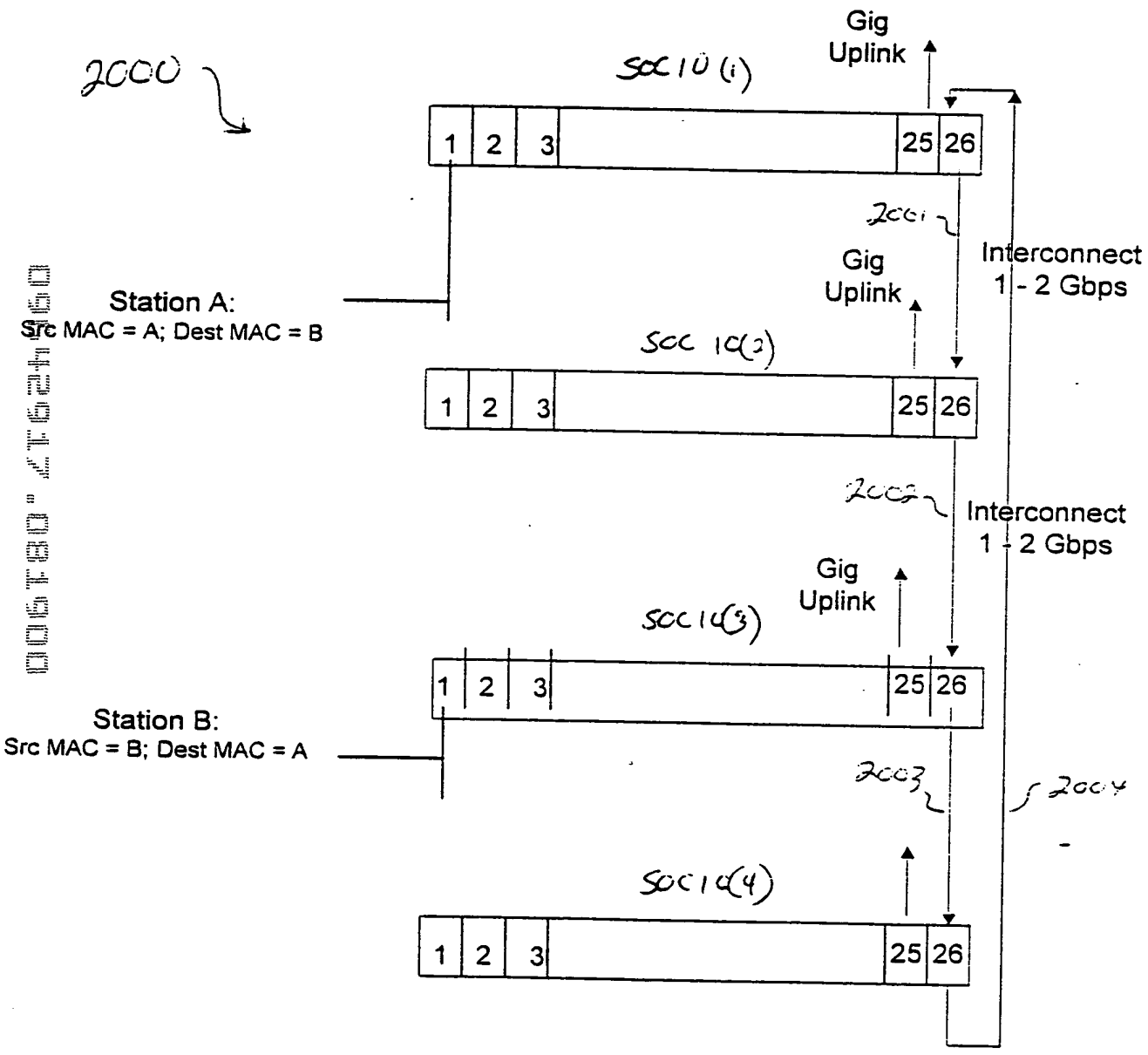

2000
SOC 10 (1)
Gig Uplink
1
2
3
25
26
2001
Interconnect 1 - 2 Gbps
Gig Uplink
SOC 10(2)
Station A:
Src MAC = A; Dest MAC = B
2002
Interconnect 1 - 2 Gbps
Gig Uplink
SOC 10(3)
Station B:
Src MAC = B; Dest MAC = A
2003
2004
SOC 10(4)

Fig 25

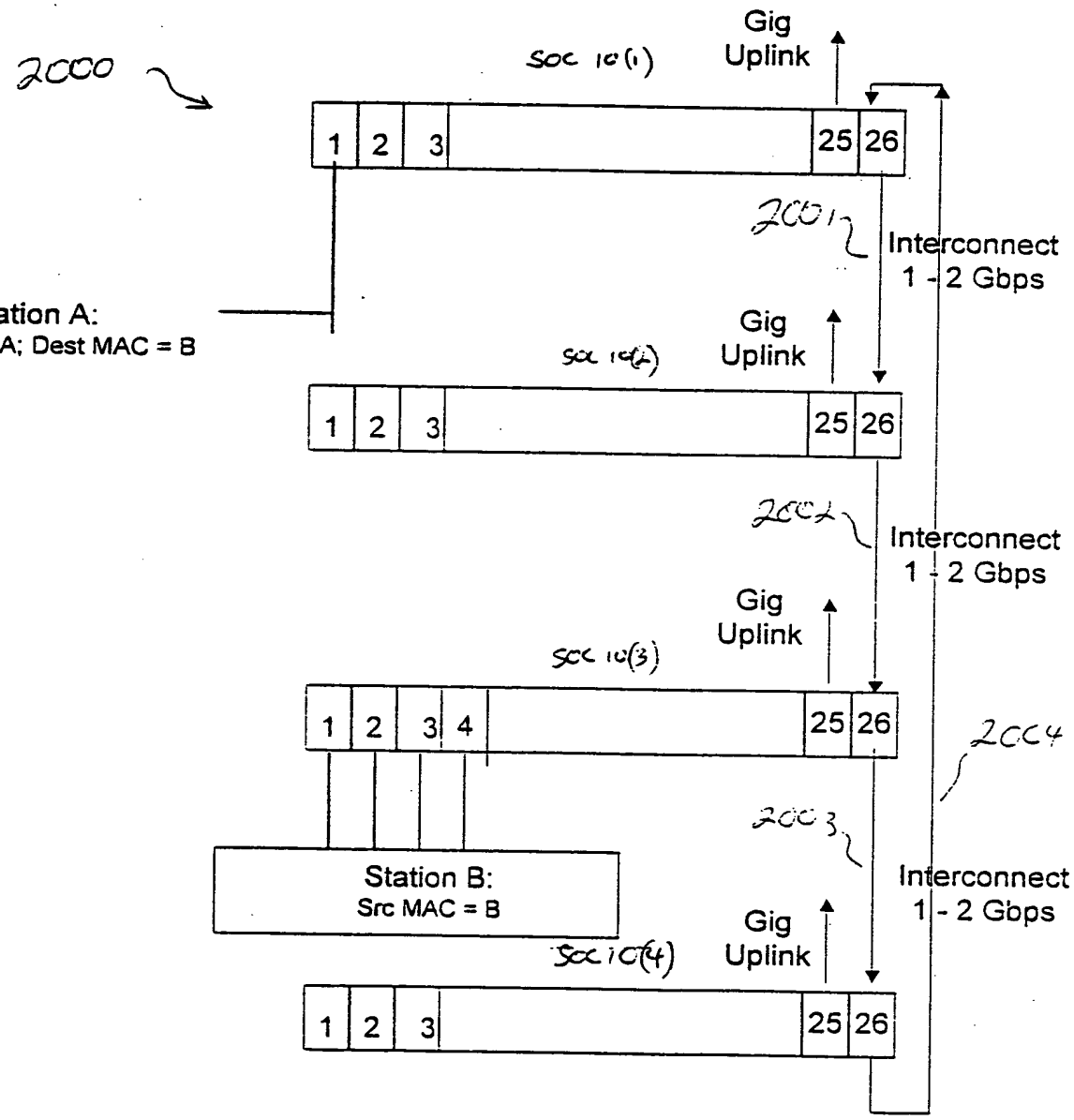

2000
SOC 10(1)
Gig Uplink
1
2
3
25
26
2001
Interconnect 1 - 2 Gbps
Station A:
Src MAC = A; Dest MAC = B
SOC 10(2)
Gig Uplink
2002
Interconnect 1 - 2 Gbps
Gig Uplink
SOC 10(3)
4
2004
2003
Station B:
Src MAC = B
Interconnect 1 - 2 Gbps
Gig Uplink
SOC 10(4)

Fig. 26

Fig. 27A

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
1	A	1	0	X	X
26	B	1	1	2	2

Fig. 27B

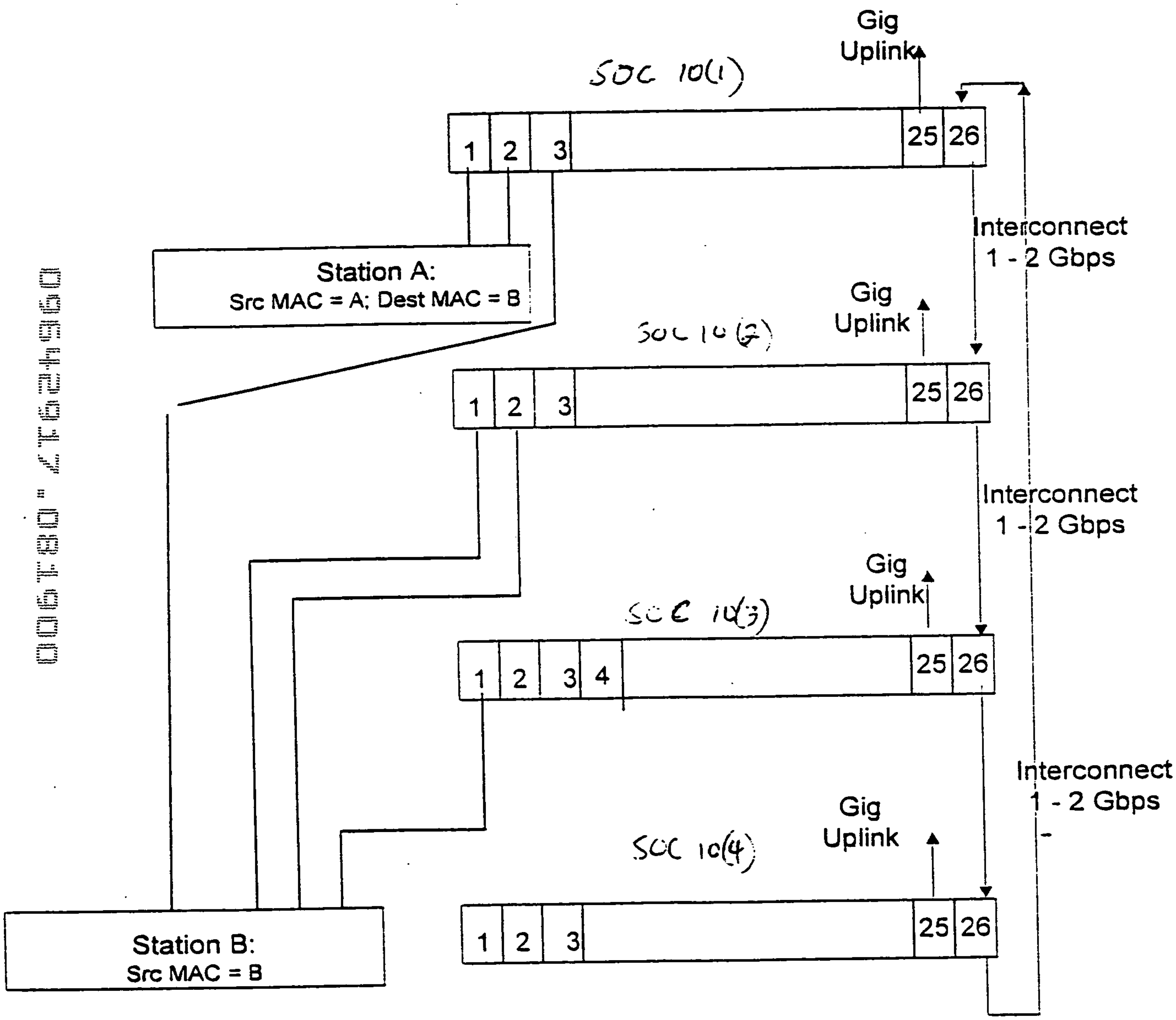
Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	0	X	X
26	B	1	1	2	2

Fig. 27C

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	0	X	X
1	B	1	1	2	2

Fig. 27D

Port Number	Mac Address	Vlan ID	T	TGID	RTAG_
26	A	1	0	X	X
26	B	1	1	2	2



Gig
Uplink
SOC 10(1)
1
2
3
25
26
Interconnect
1 - 2 Gbps
Station A:
Src MAC = A; Dest MAC = B
Gig
Uplink
SOC 10(2)
1
2
3
25
26
Interconnect
1 - 2 Gbps
Gig
Uplink
SOC 10(3)
1
2
3
4
25
26
Interconnect
1 - 2 Gbps
Gig
Uplink
SOC 10(4)
1
2
3
25
26
Station B:
Src MAC = B

Fig. 28

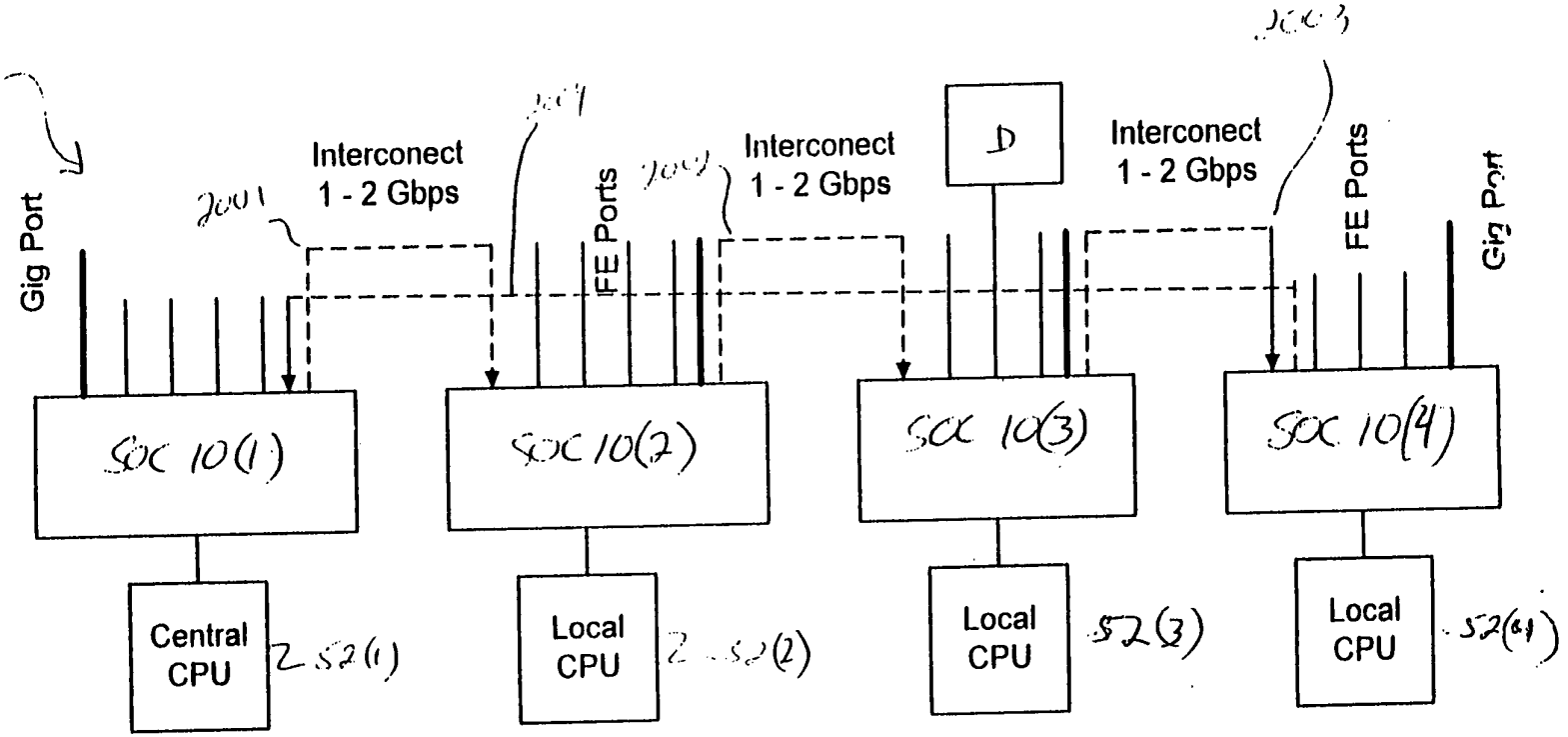

Gig Port
Interconect
1 - 2 Gbps
FE Ports
Interconect
1 - 2 Gbps
D
Interconect
1 - 2 Gbps
FE Ports
Gig Port
SOC 10(1)
SOC 10(2)
SOC 10(3)
SOC 10(4)
Central CPU
Local CPU
Local CPU
Local CPU

Fig 29

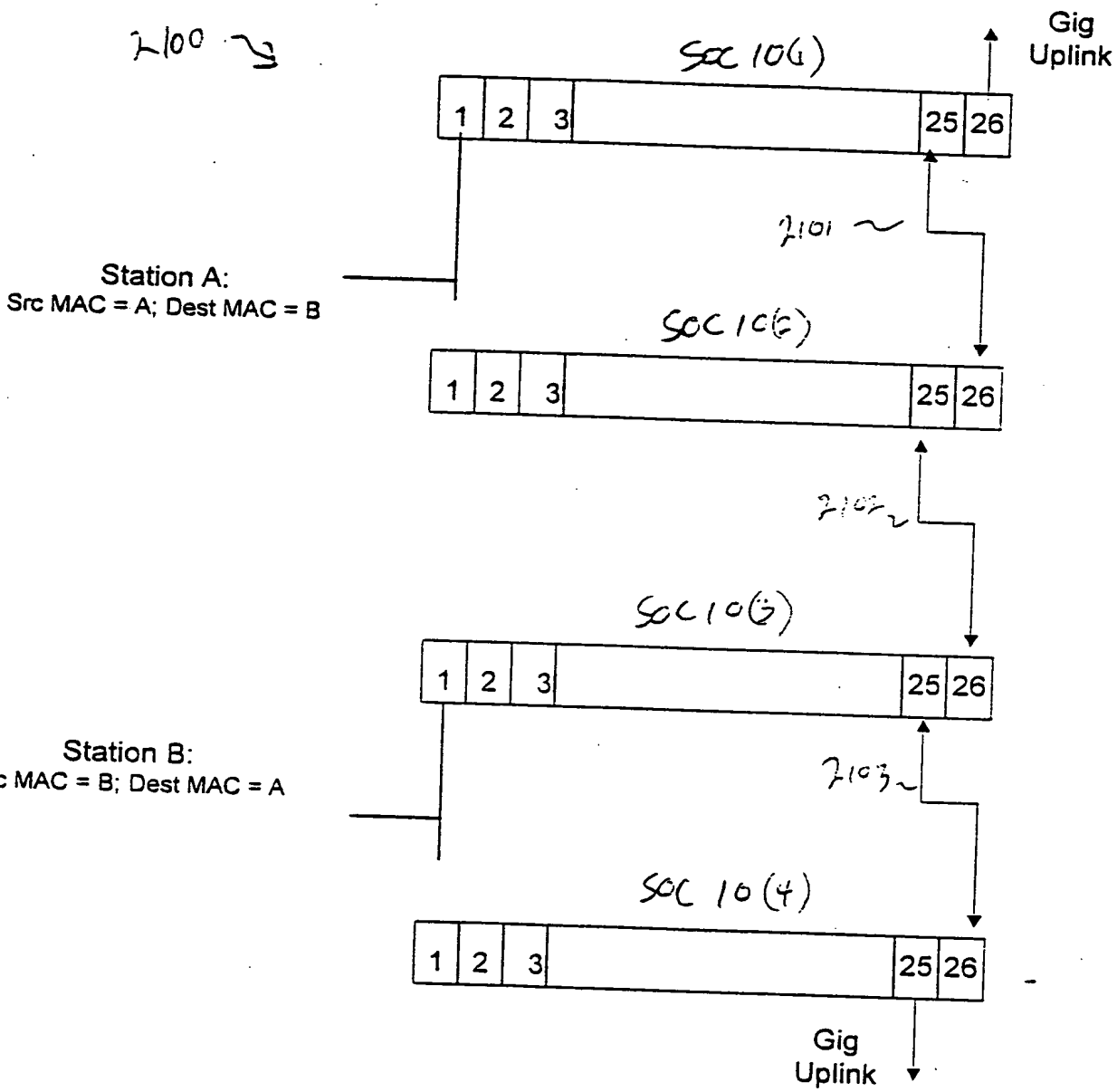

2100
SOC 10(1)
Gig Uplink
1
2
3
25
26
2101
Station A:
Src MAC = A; Dest MAC = B
SOC 10(2)
2102
SOC 10(3)
Station B:
Src MAC = B; Dest MAC = A
2103
SOC 10(4)
Gig Uplink

Fig 30

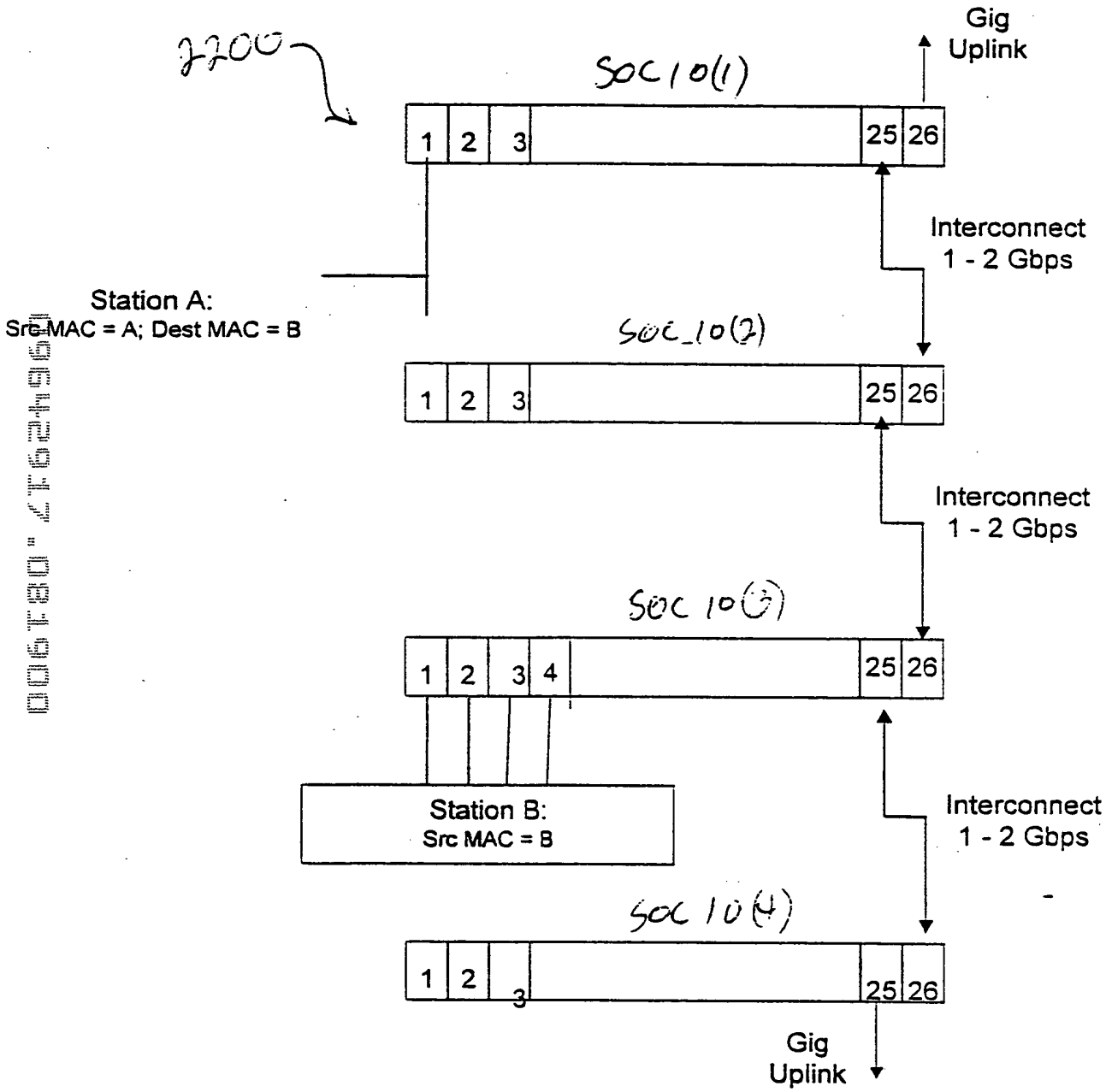

3200
SOC 10(1)
Gig Uplink
1
2
3
25
26
Interconnect 1 - 2 Gbps
Station A:
Src MAC = A; Dest MAC = B
SOC_10(2)
Interconnect 1 - 2 Gbps
SOC 10(3)
4
Station B:
Src MAC = B
Interconnect 1 - 2 Gbps
SOC 10(4)
Gig Uplink

Fig 31

Fig 32A

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
1	A	1	0	X	X
25	B	1	1	2	2

Fig 32B

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	0	X	X
25	B	1	1	2	2

Fig 32C

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	0	X	X
1	B	1	1	2	2

Fig 32D

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	0	X	X

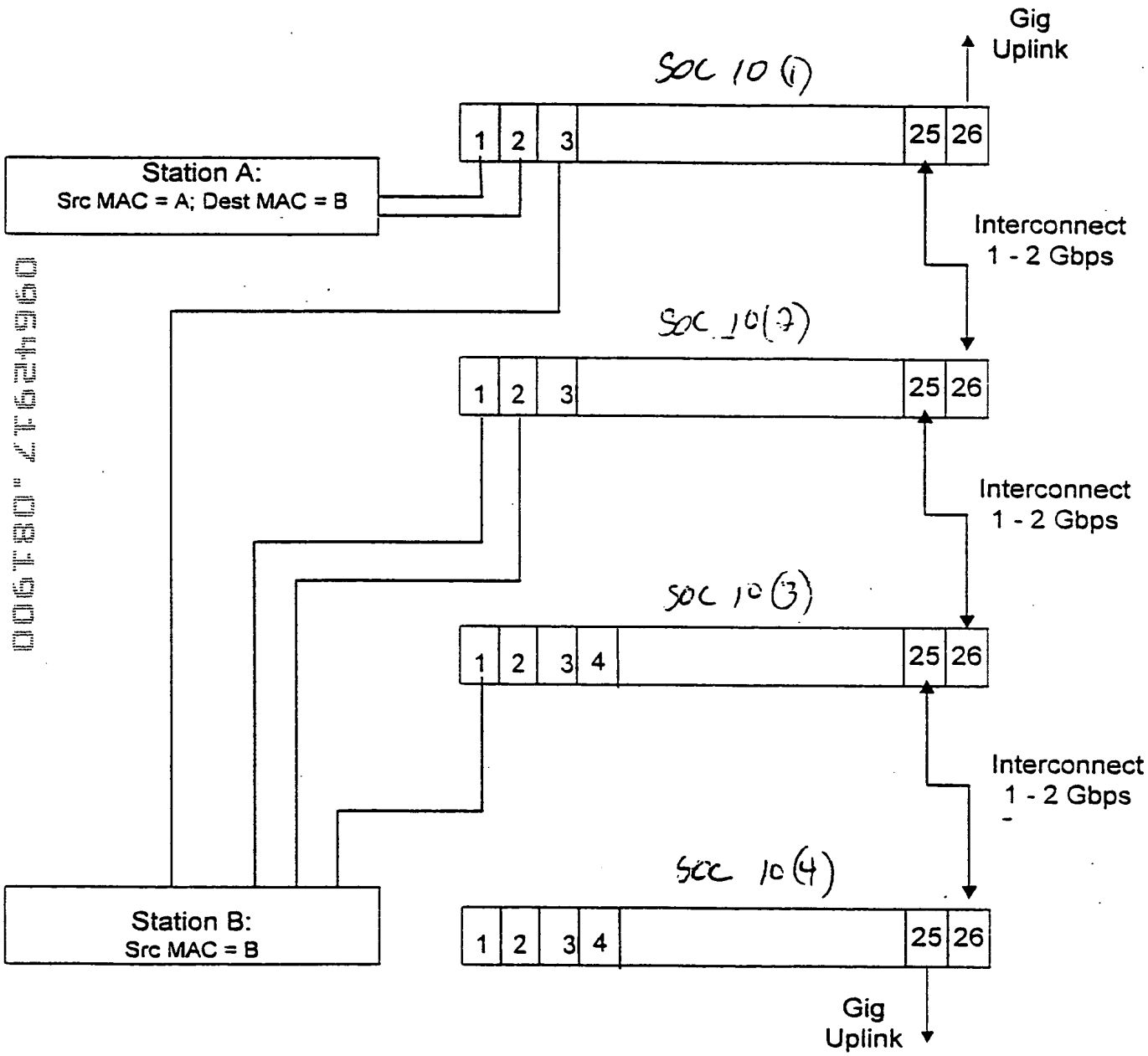

Gig
Uplink
SOC 10 (1)
1
2
3
25
26
Station A:
Src MAC = A; Dest MAC = B
Interconnect
1 - 2 Gbps
SOC 10(2)
1
2
3
25
26
Interconnect
1 - 2 Gbps
SOC 10(3)
1
2
3
4
25
26
Interconnect
1 - 2 Gbps
SOC 10(4)
1
2
3
4
25
26
Station B:
Src MAC = B
Gig
Uplink

Fig 33

Fig. 34A

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
1	A	1	1	1	1
25	B	1	1	2	2

Fig. 34B

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	1	1	1
25	B	1	1	2	2

Fig. 34C

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	1	1	1
1	B	1	1	2	2

Fig 34D

Port Number	Mac Address	Vlan ID	T	TGID	RTAG
26	A	1	1	1	1

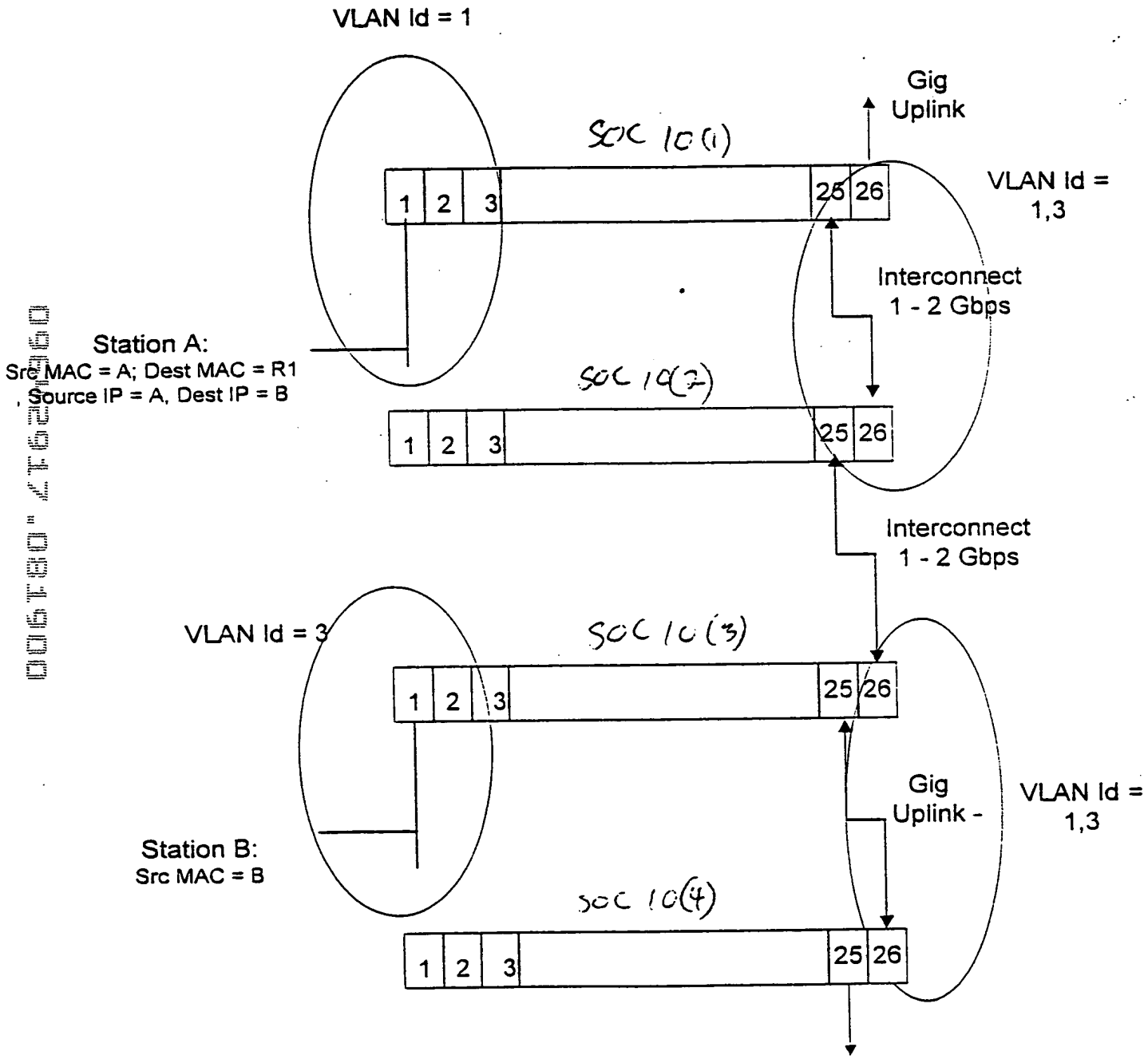

VLAN Id = 1
Gig Uplink
SOC 10(1)
1 2 3
25 26
VLAN Id = 1,3
Interconnect 1 - 2 Gbps
Station A:
Src MAC = A; Dest MAC = R1
Source IP = A, Dest IP = B
SOC 10(2)
1 2 3
25 26
Interconnect 1 - 2 Gbps
VLAN Id = 3
SOC 10(3)
1 2 3
25 26
Gig Uplink -
VLAN Id = 1,3
Station B:
Src MAC = B
SOC 10(4)
1 2 3
25 26

Fig. 35

Trunk Group Table for SW1:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
2	25	25	25	25	X	X	X	X	4

Trunk Group Table for SW2:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
2	25	25	25	25	X	X	X	X	4

Trunk Group Table for SW3:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
2	1	2	3	4	X	X	X	X	4

Trunk Group Table for SW4:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
2	26	26	26	26	X	X	X	X	4

Fig. 36

Trunk Group Table for SW1:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
1	1	2	X	X	X	X	X	X	2
2	25	25	25	3	X	X	X	X	4

Trunk Group Table for SW2:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
1	26	26	X	X	X	X	X	X	2
2	25	1	2	26	X	X	X	X	4

Trunk Group Table for SW3:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
1	26	26	X	X	X	X	X	X	2
2	1	26	26	26	X	X	X	X	4

Trunk Group Table for SW4:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG Size
1	26	26	X	X	X	X	X	X	2
2	26	26	26	26	X	X	X	X	4

Fig. 37

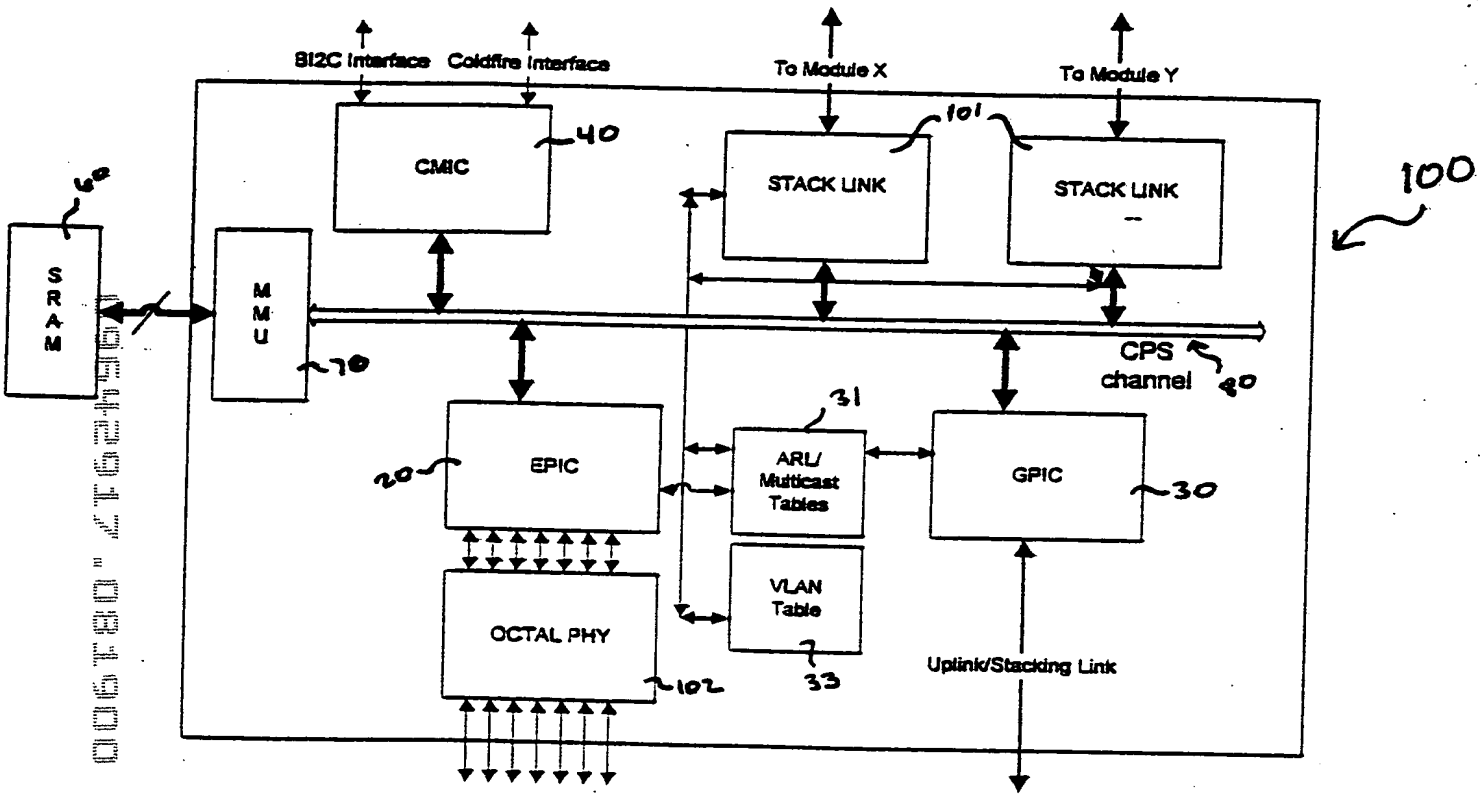

I2C Interface
Coldfire Interface
To Module X
To Module Y
CMIC
40
STACK LINK
101
STACK LINK
100
60
SRAM
MMU
70
CPS channel
80
31
EPIC
20
ARL/ Multicast Tables
GPIC
30
VLAN Table
33
OCTAL PHY
102
Uplink/Stacking Link

FIGURE 38

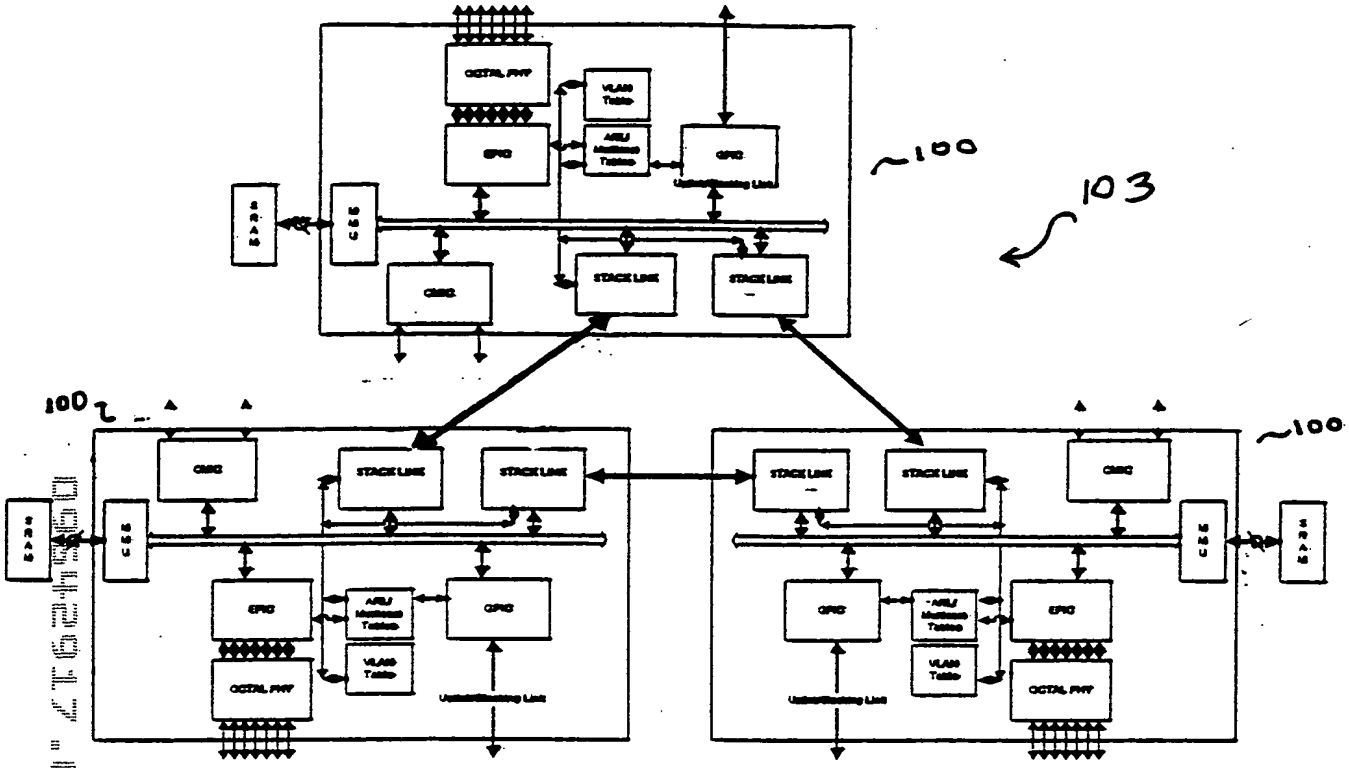


FIGURE 39

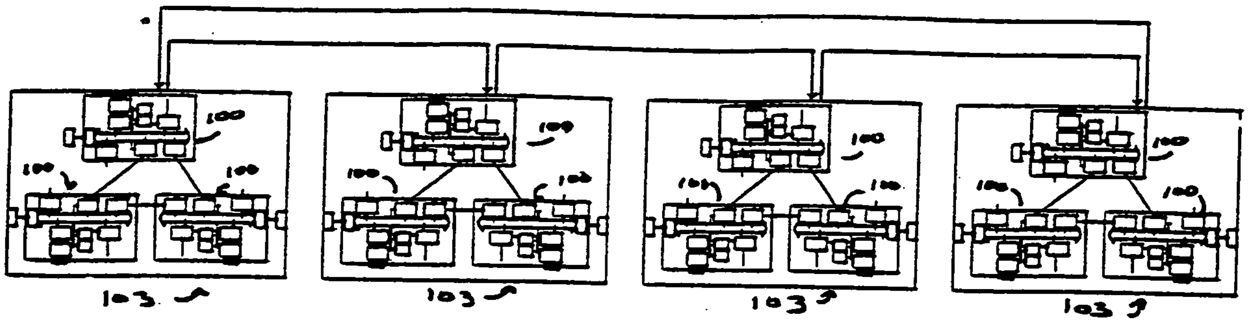


FIGURE 40

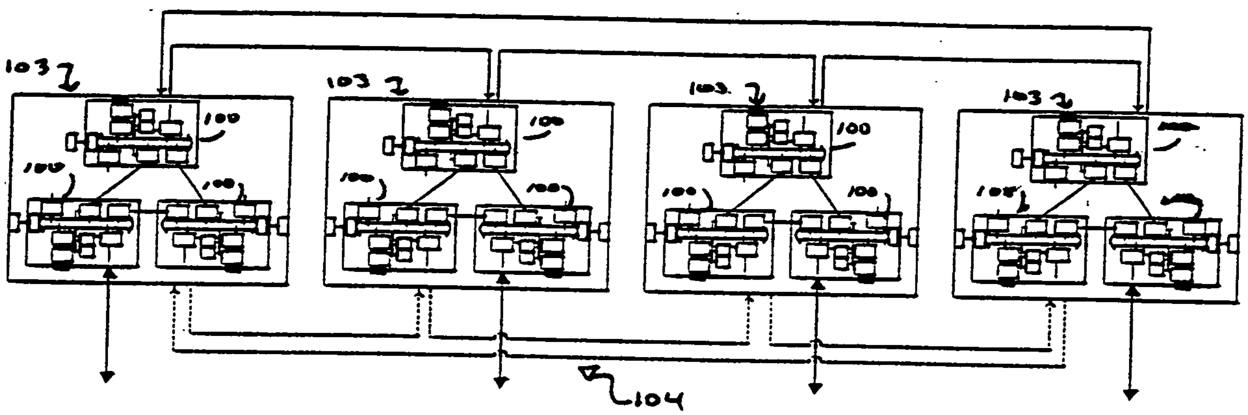


FIGURE 41

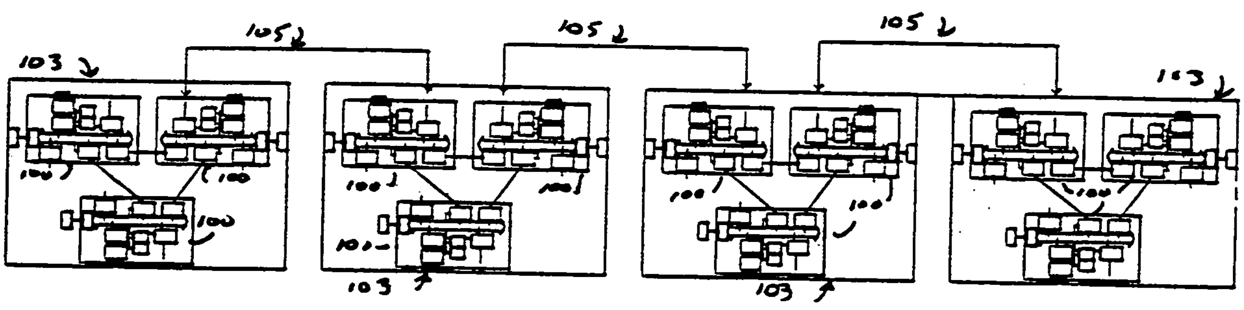


FIGURE 42

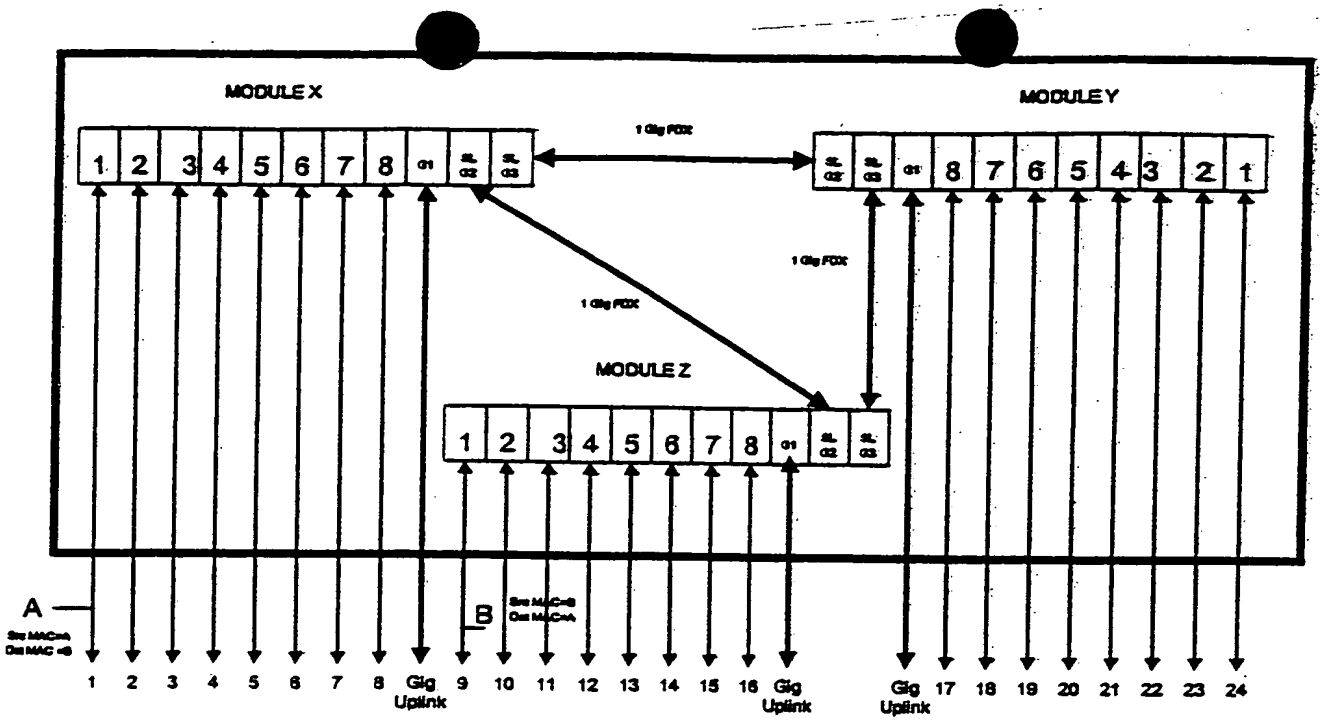


FIGURE 43

. Table for Module X

Port Number	Mac Address	Vlan ID
1	A	1

TABLE A

. Table for module Y

Port Number	Mac Address	Vlan ID
G2	A	1

TABLE B

. Table for Z

Port Number	Mac Address	Vlan ID
G2	A	1

TABLE C

Port Number	Mac Address	Vlan ID
G2	A	1
9	B	1

TABLE A

Port Number	Mac Address	Vlan ID
1	A	1
G2	B	1

TABLE B

FIGURE 44

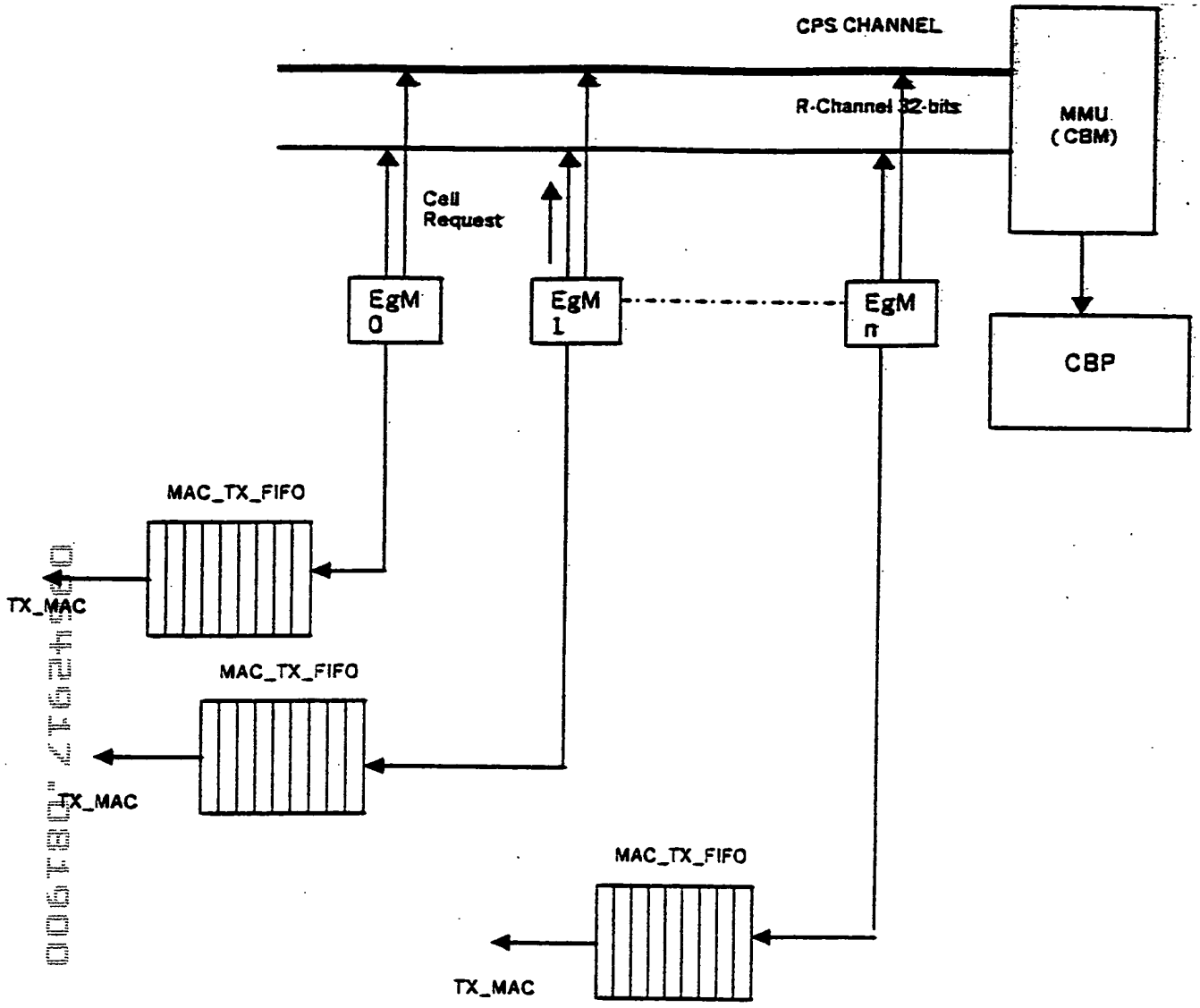

CPS CHANNEL
R-Channel 32-bits
MMU
(CBM)
Cell
Request
EgM
0
EgM
1
EgM
n
CBP
MAC_TX_FIFO
TX_MAC
MAC_TX_FIFO
TX_MAC
MAC_TX_FIFO
TX_MAC

FIGURE 45

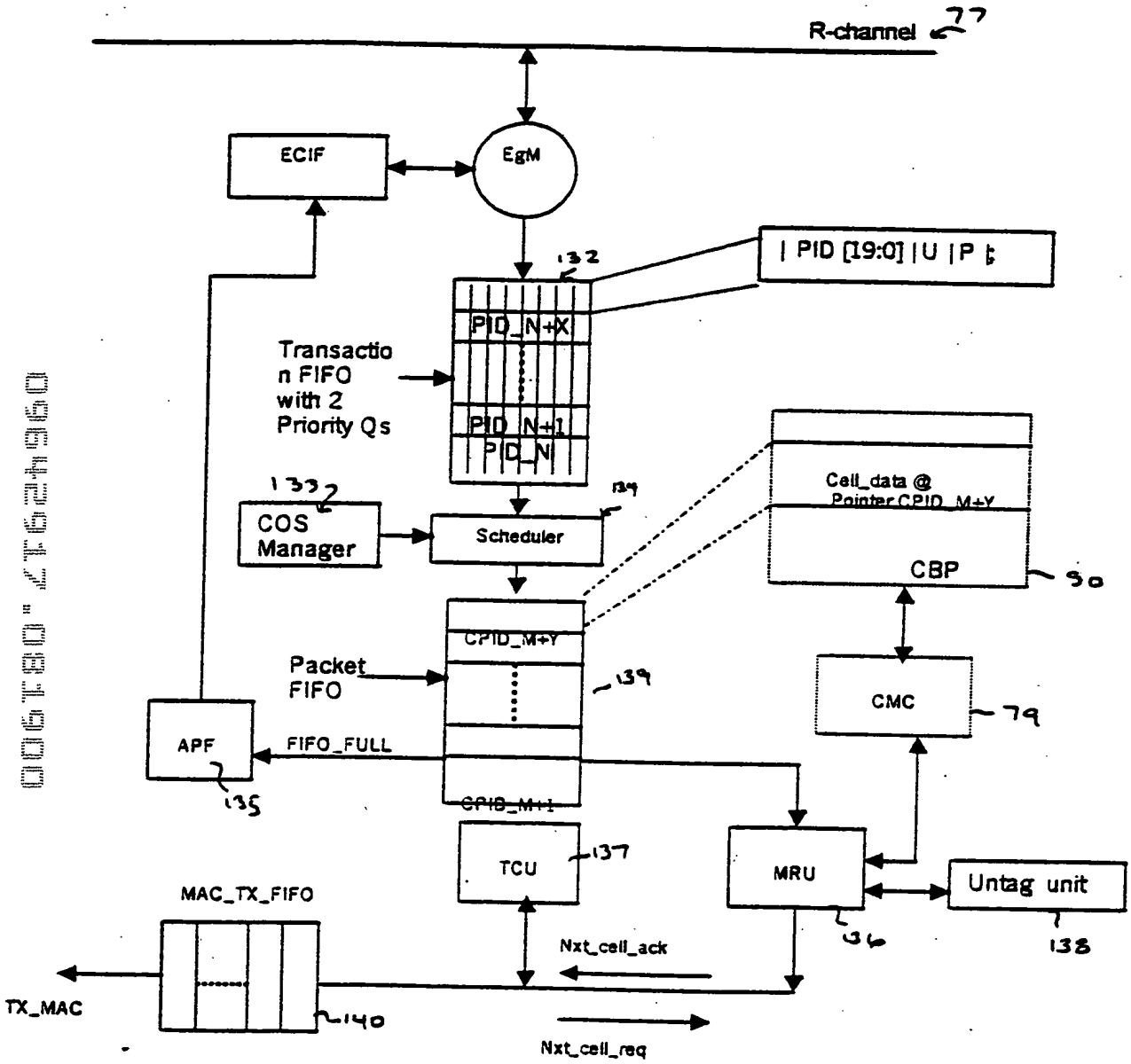

R-channel
77
ECIF
EgM
132
| PID [19:0] | U | P |
PID_N+X
PID_N+1
PID_N
Transactio
n FIFO
with 2
Priority Qs
133
COS
Manager
Scheduler
134
Cell_data @
Pointer CPID_M+Y
CBP
90
CPID_M+Y
Packet
FIFO
139
CMC
79
APF
FIFO_FULL
135
CPID_M+1
TCU
137
MRU
Untag unit
136
138
MAC_TX_FIFO
Nxt_cell_ack
TX_MAC
140
Nxt_cell_req

FIGURE 46